R&S®RTP
HIGH-PERFORMANCE OSCILLOSCOPE

Specifications

Specifications
Version 12.00

ROHDE&SCHWARZ
Make ideas real

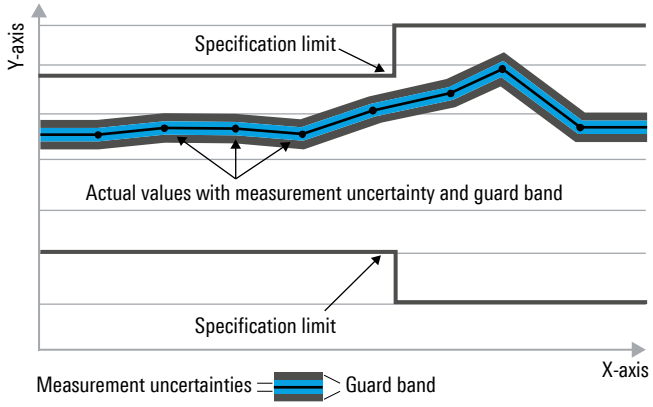
CONTENTS

Definitions

General
Product data applies under the following conditions:

- Three hours of storage at ambient temperature followed by 30 minutes of warm-up operation
- Specified environmental conditions met
- Recommended calibration interval adhered to
- All internal automatic adjustments performed, if applicable

Specifications with limits
Represent warranted product performance by means of a range of values for the specified parameter. These specifications are marked with limiting symbols such as <, ≤, >, ≥, ± or descriptions such as maximum, limit of, minimum. Compliance is ensured by testing or is derived from the design. Test limits are narrowed by guard bands to take into account measurement uncertainties, drift and aging, if applicable.



Non-traceable specifications with limits (n. trc.)
Represent product performance that is specified and tested as described under “Specifications with limits” above. However, product performance in this case cannot be warranted due to the lack of measuring equipment traceable to national metrology standards. In this case, measurements are referenced to standards used in the Rohde & Schwarz laboratories.

Specifications without limits
Represent warranted product performance for the specified parameter. These specifications are not specially marked and represent values with no or negligible deviations from the given value, e.g. dimensions or resolution of a setting parameter. Compliance is ensured by design.

Typical data (typ.)
Characterizes product performance by means of representative information for the given parameter. When marked with <, > or as a range, it represents the performance met by approximately 80 % of the instruments at production time. Otherwise, it represents the mean value.

Nominal values (nom.)
Characterize product performance by means of a representative value for the given parameter, e.g. nominal impedance. In contrast to typical data, a statistical evaluation does not take place and the parameter is not tested during production.

Measured values (meas.)
Characterize expected product performance by means of measurement results gained from individual samples.

Uncertainties
Represent limits of measurement uncertainty for a given measurand. Uncertainty is defined with a coverage factor of 2 and has been calculated in line with the rules of the Guide to the Expression of Uncertainty in Measurement (GUM), taking into account environmental conditions, aging, wear and tear.

Device settings and GUI parameters are designated with the format “parameter: value”.

Non-traceable specifications with limits, typical data as well as nominal and measured values are not warranted by Rohde & Schwarz.

In line with the 3GPP standard, chip rates are specified in million chips per second (Mcps), whereas bit rates and symbol rates are specified in billion bit per second (Gbps), million bit per second (Mbps), thousand bit per second (kbps), million symbols per second (Msps) or thousand symbols per second (ksps), and sample rates are specified in million samples per second (Msample/s). Gbps, Mcps, Mbps, Msps, kbps, ksps and Msample/s are not SI units.

Base unit

Vertical system

Input channels		4 channels
Input impedance	offset and position set to zero	50 Ω ± 2 %
Analog bandwidth (–3 dB)	R&S®RTP044B	≥ 4 GHz
	R&S®RTP064B	≥ 6 GHz
	R&S®RTP084B	≥ 8 GHz
	R&S®RTP134B	≥ 13 GHz on 2 channels [1], ≥ 8 GHz on 4 channels
	R&S®RTP164B	≥ 16 GHz on 2 channels [1], ≥ 8 GHz on 4 channels
Rise/fall time	10 % to 90 %, calculated from 0.43/analog bandwidth	
	R&S®RTP044B	108 ps
	R&S®RTP064B	72 ps
	R&S®RTP084B	54 ps
	R&S®RTP134B	33 ps
	R&S®RTP164B	27 ps
	20 % to 80 %, calculated from 0.3/analog bandwidth	
	R&S®RTP044B	75 ps
	R&S®RTP064B	50 ps
	R&S®RTP084B	38 ps
	R&S®RTP134B	23 ps
	R&S®RTP164B	19 ps
Vertical resolution		8 bit, 16 bit for high resolution decimation (with reduction of the sampling rate), 16 bit for high definition mode (without reduction of the sampling rate [2])
DC gain accuracy	offset and position set to zero	
	> 5 mV/div	±1.5 %
	≤ 5 mV/div	±2 %
Input coupling		DC
Input sensitivity	entire analog bandwidth supported for all input sensitivities	2 mV/div to 1 V/div
	in high definition mode	1 mV/div to 1 V/div
Maximum input voltage		±5 V
Position range		±5 div
Offset range	input sensitivity	
	> 100 mV/div	±5 V
	≤ 100 mV/div	±(1.5 V – input sensitivity × 5 div)
Offset accuracy	input sensitivity	
	> 100 mV/div	±(0.35 % × |net offset| + 0.1 div × input sensitivity)
	≤ 100 mV/div, net offset ≤ 1 V	±(0.35 % × |net offset| + 0.1 div × input sensitivity + 2 mV)
	≤ 100 mV/div, net offset > 1 V	±2 % × |net offset|
	net offset = offset – position × input sensitivity	
DC measurement accuracy	after adequate suppression of measurement noise	±(DC gain accuracy × |reading – net offset| + offset accuracy)
Amplitude accuracy	DC to 90 % of analog bandwidth	
	≤ 8 GHz	< 0.5 dB (typ.)
	> 8 GHz	< 0.75 dB (typ.)
Phase accuracy	maximum deviation from best fit line	
	over full analog bandwidth	< 3° (typ.)
	within any 500 MHz span	< 1° (typ.)
Channel-to-channel isolation (each channel at same input sensitivity)	between channels 1-3, 1-4, 2-3, 2-4	> 60 dB (typ.)
	between channels 1-2 and 3-4	> 40 dB (typ.)

[1] Two channels mean either channel 1 or channel 2 and either channel 3 or channel 4.

[2] The maximum realtime sampling rate of the high definition mode is 10 Gsample/s.

RMS noise floor (meas.) (corresponding signal to noise ratio at full scale (calculated))	input sensitivity	**R&S®RTP044B**	**R&S®RTP064B**
	2 mV/div	270 µV (28.3 dB)	340 µV (26.3 dB)
	5 mV/div	280 µV (36.0 dB)	360 µV (33.8 dB)
	10 mV/div	410 µV (38.7 dB)	500 µV (37.0 dB)
	20 mV/div	630 µV (41.0 dB)	750 µV (39.5 dB)
	50 mV/div	1.4 mV (42.0 dB)	1.7 mV (40.3 dB)
	100 mV/div	2.7 mV (42.3 dB)	3.1 mV (41.1 dB)
	200 mV/div	6.6 mV (40.6 dB)	8.2 mV (38.7 dB)
	500 mV/div	14 mV (42.0 dB)	17 mV (40.3 dB)
	1 V/div	27 mV (42.3 dB)	32 mV (40.9 dB)
	input sensitivity	**R&S®RTP084B**	**R&S®RTP134B**
	2 mV/div	430 µV (24.3 dB)	670 µV (20.5 dB)
	5 mV/div	440 µV (32.1 dB)	720 µV (27.8 dB)
	10 mV/div	620 µV (35.1 dB)	900 µV (31.9 dB)
	20 mV/div	880 µV (38.1 dB)	1.3 mV (34.7 dB)
	50 mV/div	2.0 mV (38.9 dB)	2.7 mV (36.3 dB)
	100 mV/div	3.6 mV (39.8 dB)	4.3 mV (38.3 dB)
	200 mV/div	9.8 mV (37.2 dB)	12 mV (35.4 dB)
	500 mV/div	21 mV (38.5 dB)	27 mV (36.3 dB)
	1 V/div	36 mV (39.8 dB)	43 mV (38.3 dB)
	input sensitivity	**R&S®RTP164B**	
	2 mV/div	840 µV (18.5 dB)	
	5 mV/div	900 µV (25.9 dB)	
	10 mV/div	1.15 mV (29.8 dB)	
	20 mV/div	1.5 mV (33.5 dB)	
	50 mV/div	3.4 mV (34.3 dB)	
	100 mV/div	5.2 mV (36.6 dB)	
	200 mV/div	14 mV (34.1 dB)	
	500 mV/div	32 mV (34.8 dB)	
	1 V/div	48 mV (37.3 dB)	

Horizontal system

Timebase range		10 ps/div to 10 000 s/div, settable to any value within range
Reference position	horizontal position of trigger point	0 % to 100 % of measurement display area
Horizontal position range	max.	+(memory depth/current sampling rate)
	min.	–10 000 s
Horizontal modes	normal mode	if timebase < 1 s/div (default value) or roll mode = off
	roll mode	The acquired waveform points are continuously scrolled from the right to the left of the display. Sample rates up to 20 Msample/s with a maximum record length of 40 Mpoints are supported.
Channel-to-channel skew		< 10 ps (meas.)
Deskew range		–100 ns to +100 ns in steps of 10 fs
Timebase accuracy	after delivery/calibration, at +23 °C	±10 ppb
	during calibration interval	±100 ppb
	long-term stability (more than one year since calibration)	±(50 + 50 × years since calibration) ppb
Sample clock jitter	acquired time range	RMS value (meas.)
	1 µs	50 fs
	10 µs	63 fs
	100 µs	72 fs
	1 ms	76 fs
	10 ms	124 fs
Intrinsic jitter	RMS value	200 fs (meas.)
Time interval error (TIE)	RMS values	$\sqrt{(\text{Noise}/\text{SlewRate})^2 + (\text{Intrinsic Jitter})^2}$
Periodic jitter	RMS values	$\sqrt{2}\sqrt{(\text{Noise}/\text{SlewRate})^2 + (\text{Intrinsic Jitter})^2}$
Cycle-to-cycle jitter	RMS values	$\sqrt{3}\sqrt{(\text{Noise}/\text{SlewRate})^2 + (\text{Intrinsic Jitter})^2}$

Delta time accuracy	intra channel, peak-to-peak, ±5 sigma	$\pm\left(5 \cdot \sqrt{\mathrm{TIE}_{\mathrm{edge1}}{}^2 + \mathrm{TIE}_{\mathrm{edge2}}{}^2} + \text{timebase accuracy} \cdot \text{delta time}\right)$

Acquisition system

Realtime sampling rate		max. 20 Gsample/s on 4 channels, max. 40 Gsample/s on 2 channels
Realtime waveform acquisition rate	max.	> 750 000 waveforms/s
Memory depth [3]	standard	100 Mpoints on 4 channels
		200 Mpoints on 2 channels
		400 Mpoints on 1 channel
	R&S®RTP-B102 option	200 Mpoints on 4 channels
		400 Mpoints on 2 channels
		800 Mpoints on 1 channel
	R&S®RTP-B105 option	500 Mpoints on 4 channels
		1 Gpoints on 2 channels
		2 Gpoints on 1 channel
	R&S®RTP-B110 option	1 Gpoints on 4 channels
		2 Gpoints on 2 channels
		3 Gpoints on 1 channel
	R&S®RTP-B120 option	2 Gpoints on 4 channels
		3 Gpoints on 2 channels
		3 Gpoints on 1 channel
	R&S®RTP-B130 option	3 Gpoints on 4 channels
		3 Gpoints on 2 channels
		3 Gpoints on 1 channel
Realtime digital filters	selectable for the data acquisition and/or the trigger system	
	lowpass for acquisition system	cutoff frequency selectable from 100 kHz to 500 MHz
	lowpass for acquisition and trigger system	cutoff frequency selectable from 1 GHz to the analog bandwidth with fine granularity
Decimation modes	sample	first sample in decimation interval
	peak detect	largest and smallest sample in decimation interval
	high resolution	average value of samples in decimation interval
	root mean square	root of squared average of samples in decimation interval
Waveform arithmetic	off	no arithmetic
	envelope	envelope of acquired waveforms
	average	average of acquired waveforms, max. average depth depends on decimation mode [4]
	sample	max. 16 777 215
	high resolution	max. 65 535
	root mean square	max. 255
	reset condition	no reset (standard), reset by time, reset by number of processed waveforms
Waveform streams per channel		up to 3 with independent selection of decimation mode and waveform arithmetic
Sampling modes	realtime mode	max. sampling rate set by digitizer
	interpolated time	enhancement of sampling resolution by interpolation; max. equivalent sampling rate is 10 Tsample/s
Interpolation modes		linear, sin(x)/x, sample & hold

[3] The maximum available memory depth depends on the bit depth of the acquired data and, therefore, on the settings of the acquisition system, such as decimation mode, waveform arithmetic, number of waveform streams and high definition mode.

[4] Waveform averaging is not compatible with peak detect decimation.

Fast segmentation mode	continuous recording of waveforms in acquisition memory without interruption due to visualization	
	max. realtime waveform acquisition rate	> 3 000 000 waveforms/s
	min. blind time between consecutive acquisitions	< 350 ns
	max. recordable acquisitions	up to 1.5 million acquisitions, depending on instrument settings and memory option (R&S®RTP-B102/-B105/ -B110/-B120/-B130)
History mode	accesses previous acquisitions for further analysis	
	max. recordable acquisitions	up to 1.5 million acquisitions, depending on instrument settings and memory option (R&S®RTP-B102/-B105/ -B110/-B120/-B130)
	analysis functions	same as for the waveform of the latest acquisition: waveform measurements, mask testing, waveform math, search and mark functions, zoom and others
	history player	shows one history acquisition after the other for a user definable display time (40 µs to 10 s)
	timestamp formats	timestamp of each acquisition: absolute (date and time) or relative to latest acquisition
	save options	all history acquisitions or a user definable subset

Differential signals

General description	Calculation of differential and common mode signals from p part and n part connected to separate input channels. Because of the R&S®RTP digital trigger concept, these signals can be used as a trigger input.	
Input channels		channel 1, channel 2, channel 3, channel 4
Differential signal		difference between any two input channels
Common mode signal		sum of any two input channels
Maximum number of outputs [5]	differential signals	2
	common mode signals	2

High definition mode

General description	The high definition mode increases the numeric resolution of the waveform signal by using digital filtering, leading to a reduced noise. Because of the R&S®RTP digital trigger concept, the signals with increased numeric resolution are used as input for triggering.	
Numeric resolution	bandwidth	resolution
	10 kHz to 200 MHz	16 bit
	300 MHz	12 bit
	500 MHz	12 bit
	1 GHz	11 bit
	2 GHz	10 bit
Realtime sampling rate		max. 10 Gsample/s on each channel

Trigger system

Sources		channel 1, channel 2, channel 3, channel 4, inverted channels, external trigger, line trigger, differential, common mode
Trigger bandwidth	max.	same bandwidth as analog bandwidth for all vertical scales and trigger types
	user-defined	1 GHz to analog bandwidth

[5] Together with R&S®RTP-K122 realtime deembedding extension, only one output can be calculated, differential or common mode.

Trigger sensitivity		0.0001 div, from DC to analog bandwidth for all vertical scales and trigger types
Trigger hysteresis	modes	auto (standard) or manual
	sensitivity	0.0001 div, from DC to analog bandwidth for all vertical scales and trigger types
Trigger jitter	full-scale sine wave of frequency set to –3 dB bandwidth	< 80 fs (RMS) (meas.)
Sweep mode		auto, normal, single, n single
Event rate	max.	one event for every 200 ps time interval
Trigger level range	internal	±5 div from center of screen
	external	see External trigger input
Holdoff range	time	100 ns to 10 s, fixed and random
	events	1 event to 2 000 000 000 events

Main trigger modes		
Edge	triggers on specified slope (positive, negative or either) and level	
Glitch	triggers on glitches of positive, negative or either polarity that are shorter or longer than specified width	
	glitch width	25 ps to 10 000 s
Width	triggers on positive or negative pulse of specified width; width can be shorter, longer, inside or outside the interval	
	pulse width	25 ps to 10 000 s
Runt	triggers on pulse of positive, negative or either polarity that crosses one threshold but fails to cross a second threshold before crossing the first one again; runt pulse width can be arbitrary, shorter, longer, inside or outside the interval	
	runt pulse width	25 ps to 10 000 s
Window	triggers when signal enters or exits a specified voltage range; triggers also when signal stays inside or outside the voltage range for a specified period of time	
Timeout	triggers when signal stays high, low or unchanged for a specified period of time	
	timeout	25 ps to 10 000 s
Interval	triggers when time between two consecutive edges of same slope (positive or negative) is shorter, longer, inside or outside a specified range	
	interval time	25 ps to 10 000 s
Slew rate	triggers when the time required by a signal edge to toggle between user-defined upper and lower voltage levels is shorter, longer, inside or outside the interval; edge slope may be positive, negative or either	
	toggle time	25 ps to 10 000 s
Data2clock	triggers on setup time and hold time violations between clock and data present on any two input channels; monitored time interval may be specified by the user in the range from –100 ns to 100 ns around a clock edge and must be at least 100 ps wide	
Pattern	triggers when a logical combination (and, nand, or, nor) of the input channels stays true for a period of time shorter, longer, inside or outside a specified range	
State	triggers when a logical combination (and, nand, or, nor) of the input channels stays true at a slope (positive, negative or either) in one selected channel	

Advanced trigger modes		
Trigger qualification	trigger events may be qualified by a logical combination of unused channels	
	qualifiable events	edge, glitch, width, runt, window, timeout, interval
Sequence trigger (A/B/R trigger)	triggers on B event after occurrence of A event; delay condition after A event specified either as time interval or number of B events; an optional R event resets the trigger sequence to A	
	A event	any trigger mode
	B event	edge, glitch, width, runt, window, timeout, interval, slew rate
	R event	edge, glitch, width, runt, window, timeout, interval, slew rate
Zone trigger		with R&S®RTP-K19 option
CDR trigger		with R&S®RTP-K136/-K137 option
External trigger input	input impedance	50 Ω (nom.)
	max. input voltage	5 V (RMS)
	trigger level range	±5 V
	sensitivity, for input frequency ≤ 500 MHz	300 mV (peak-to-peak)
	input coupling	50 Ω, GND, HF reject (attenuates > 50 kHz), LF reject (attenuates < 50 kHz)
	trigger modes	edge (rise or fall)
Trigger out	functionality	a pulse is generated for every acquisition trigger event
	output voltage	0 V to 5 V at high impedance
		0 V to 2.5 V at 50 Ω
	pulse width	selectable between 4 ns and 60 ms
	pulse polarity	low active or high active
	output delay	depends on trigger settings
	jitter	±40 ps (RMS) (meas.)

RF characteristics [6]

Sensitivity/noise density	at 1.001 GHz (measurement of the power spectral density at 1.001 GHz at input sensitivity 2 mV/div, corresponding to –30 dBm input range of the oscilloscope, using the FFT with center frequency 1.001 GHz, span 500 kHz, RBW 3 kHz)	–157 dBm (1 Hz) (meas.)
Noise figure	at 1.001 GHz (calculated based on the noise density above)	17 dB (meas.)
Dynamic range	measured for an input carrier with frequency 1 GHz and level –1 dBm at input sensitivity 70 mV/div, corresponding to 0 dBm input range of the oscilloscope, using the FFT with center frequency 1 GHz, span 100 MHz, RBW 400 Hz at +20 MHz from the center frequency	107 dB (meas.)
Absolute amplitude accuracy	input frequency	
	≤ 12 GHz	±0.25 dB (meas.)
	> 12 GHz to ≤ 15 GHz	±0.5 dB (meas.)
Phase noise	at 1 GHz	
	10 kHz offset	–118 dBc (1 Hz) (meas.)
	100 kHz offset	–126 dBc (1 Hz) (meas.)
EVM	802.11, 20 MHz bandwidth, 64QAM	
	802.11n, 2.4 GHz carrier	–46 dB (meas.)
	802.11ac, 5.7 GHz carrier	–44 dB (meas.)

[6] The RF characteristics are measured for an R&S®RTP164B oscilloscope with 16 GHz bandwidth at zero offset.

Spurious-free dynamic range (excl. harmonics)	measured for an input carrier with frequency 950 MHz and level –1 dBm at input sensitivity 70 mV/div, corresponding to 0 dBm input range of the oscilloscope, using the FFT with center frequency 3 GHz, span 5 GHz, RBW 100 kHz	66 dB (meas.)
Second harmonic distortion	measured for an input carrier with frequency 950 MHz and level –1 dBm at input sensitivity 70 mV/div, corresponding to 0 dBm input range of the oscilloscope, using the FFT with center frequency 3 GHz, span 5 GHz, RBW 100 kHz	–52 dBc (meas.)
Third harmonic distortion	measured for an input carrier with frequency 950 MHz and level –1 dBm at input sensitivity 70 mV/div, corresponding to 0 dBm input range of the oscilloscope, using the FFT with center frequency 3 GHz, span 5 GHz, RBW 100 kHz	–43 dBc (meas.)
Third order intercept point (TOI)	measured for two input tones with frequencies 2.436 GHz and 2.438 GHz and level 0 dBm at input sensitivity 160 mV/div, corresponding to 8 dBm input range of the oscilloscope, using the FFT with center frequency 2.437 GHz, span 10 MHz, RBW 30 kHz	23.5 dBm (meas.)
Input VSWR	input frequency	
	≤ 4 GHz	1.25 (meas.)
	> 4 GHz to ≤ 16 GHz	1.4 (meas.)

Waveform measurements

General features	measurement panels	up to 8 measurement panels; each panel may contain any number of automatic measurements of the same category
	gate	delimits the display region evaluated for automatic measurements
	reference levels	user-configurable vertical levels define support structures for automatic measurements
	statistics	displays maximum, minimum, mean, standard deviation, RMS and measurement count for each automatic measurement
	track	measurement results displayed as continuous trace that is time-correlated to the measurement source
	long-term analysis	history of selected measurements as trace against count index
	histogram	available for the main measurement of each measurement panel; automatic or manual selection of bin number and scale; counters for measurements under, within and over the histogram range
	limit check	measurements tested against user-defined margins and limits; pass or fail conditions may launch automatic response: acquisition stop, beep, print and save waveform

Measurement category	amplitude and time	amplitude, high, low, maximum, minimum, peak-to-peak, mean, RMS, sigma, overshoot, area, rise time, fall time, positive width, negative width, period, frequency, duty cycle, delay, phase, burst width, pulse count, positive switching, negative switching, cycle area, cycle mean, cycle RMS, cycle sigma, setup/hold time, setup/hold ratio, pulse train, slew rate rising, slew rate falling, DC voltmeter (requires Rohde & Schwarz active probe with R&S®ProbeMeter functionality)
	eye diagram	extinction ratio, eye height, eye width, eye top, eye base, crossing points, Q factor, Noise (RMS), S/N ratio, duty cycle distortion, eye rise time, eye fall time, eye bit rate, eye amplitude, jitter (peak-to-peak, 6-sigma, RMS)
	optical	optical average power, optical modulation amplitude
	spectrum	channel power, bandwidth, occupied bandwidth, harmonic search, total harmonic distortion THD in dB and % using power values, total harmonic distortion variants THD_a, THD_u and THD_r using voltage, overall voltage and overall voltage root means square, peak list (THD_a, THD_u and THD_r require R&S®RTP-K37 option)
	jitter	cycle-to-cycle jitter, N-cycle jitter, cycle-to-cycle width, cycle-to-cycle duty cycle, time-interval error, data rate, unit interval, skew delay, skew phase; requires R&S®RTP-K12 option
Cursors	setup	up to 4 cursor sets on screen, each set consisting of two horizontal and two vertical cursors
	target	acquired waveforms (input channels), math waveforms, reference waveforms, track waveforms, XY diagrams
	operating mode	vertical measurements, horizontal measurements or both; vertical cursors either set manually or locked to waveform
Histogram	source	acquired waveform (input channels), math waveform, reference waveform
	mode	vertical (for timing statistics), horizontal (for amplitude statistics)
	automatic measurements	waveform count, waveform samples, histogram samples, histogram peak, peak value, maximum, minimum, median, range, mean, sigma, mean ± 1, 2 and 3 sigma, marker ± probability

Mask testing

Test definition	number of masks	up to 8 simultaneously
	source	acquired waveforms (input channels), math waveforms
	fail condition	sample hit or waveform hit
	fail tolerance	minimum number of fail events for test fail in range from 0 to 4 000 000 000
	test rate	up to 600 000 waveforms/s
	action on error	acquisition stop, beep, print and save waveform
	save/load to file	test and mask settings (.xml format)

Mask definition with segments	number of independent segments	up to 8
	segment definition	array of points and connecting rule (upper, lower, inner) define segment region
	segment input	point and click on touchscreen, editable list
Mask definition with tolerance tube	input signal	acquired waveform
	definition of tolerance tube	horizontal width, vertical width, vertical stretch, vertical position
Mask definition with eye mask assistant (requires one of the following options: R&S®RTP-K12/-K91/-K93/-K133/-K134/ -K136/-K137)	primary mask shape	
	type	diamond, square, hexagon, octagon
	dimensions	main and secondary height, main and secondary width, depending on selected shape
	position	vertical offset, horizontal offset
	secondary mask shapes	
	locations	any combination of left, right, top, bottom
	position	horizontal and vertical offset with respect to center of primary mask shape
Serial standard masks	multiple predefined protocol masks	D-PHY, M-PHY, C-PHY, PCIe, USB, HDMI, JESD204C, ITU and Ethernet
Result statistics	category	completed acquisitions, remaining acquisitions, state, sample hits, mask hits, fail rate, test result (pass or fail)
Visualization options	waveform style	vectors, dots
	violation highlighting	hits (on/off), highlight persistence (50 ms to 50 s or infinite), waveform color (default: red)
	mask colors	configurable colors for mask without violation (default: translucent gray), mask with violation (default: translucent red), mask with contact (default: translucent pale red)

Waveform math

General features	number of math waveforms	up to 8
	number of reference waveforms	up to 4
	waveform arithmetic	user-selectable average or envelope of consecutive waveforms
Algebraic expressions	user may define complex mathematical expressions involving waveforms and measurement results	
	math functions	add, subtract, multiply, divide, absolute value, square, square root, integrate, differentiate, exp, $\log_{10}$, $\log_e$, $\log_2$, rescale, sin, cos, tan, arcsin, arccos, arctan, sinh, cosh, tanh, autocorrelation, crosscorrelation
	logical operators	not, and, nand, or, nor, xor, nxor
	relational operators	Boolean result of =, ≠, >, <, ≤, ≥
	frequency domain	spectral magnitude and phase, real and imaginary spectra, group delay
	digital filter	lowpass, highpass or user-defined filter (specified by up to 1 million FIR filter coefficients)
	special functions	CDR transform; requires R&S®RTP-K12 option
Optimized math	operators	add, subtract, multiply, invert, absolute value, differentiate, $\log_{10}$, $\log_e$, $\log_2$, rescale, FIR, FFT magnitude

Spectrum analysis

General description	spectrum analysis allows signal analysis in the frequency domain	
Spectrum	sources	channel 1, channel 2, channel 3, channel 4
	spectrum types	magnitude spectrum, phase spectrum
	setup parameters	center frequency, frequency span, automatic RBW, resolution bandwidth, gate position, gate width, vertical scale, vertical position, frame overlap
	scaling	
	magnitude spectrum	linear, dB, dBm, dBµV, dBmV, dBV, dBps, dBns, dBµs, dBms, dBs, dBHz, dBkHz, dBMHz, dBGHz, dBµA, dBmA, dBA
	phase spectrum	degrees, radians
	frequency range	DC to Nyquist frequency (1/2 sample rate, e.g. 20 GHz at 40 Gsample/s)
	frequency axis scaling	linear or logarithmic
	span	1 Hz to 20 GHz
	resolution bandwidth	≤ 1 Hz to 2 GHz
	window types	rectangular, Hamming, Hann, Blackman Harris, Gaussian, Flattop, Kaiser Bessel
	trace types	normal, envelope, average, RMS, min. hold, max. hold
	spectrum measurements	channel power, bandwidth, occupied bandwidth, various THD variants (total harmonic distortion), harmonic search, peak list (with user definable threshold)
	max. realtime waveform acquisition rate	> 1000 waveforms/s
	spectrogram	requires R&S®RTP-K37 option

Search and mark function

General description	scans acquired waveforms for occurrence of a user-defined set of events and highlights each occurrence	
Basic setup	source	all physical input channels, math waveforms, reference waveforms
	search panels	up to 8, where each panel may manage multiple event searches
	search mode	manually triggered or continuous
	search conditions	
	supported events	edge, glitch, width, runt, window, timeout, interval, slew rate, data2clock, state
	event configuration	identical to corresponding trigger event
	event selection	single or multiple events on same source
Search oscilloscope	mode	current waveform, gated time interval
Result visualization	table	
	sort mode	horizontal position or vertical value
	max. result count	specifies max. table size
	zoom window	centered on highlighted event

Display characteristics

Diagram types	Yt, XY, spectrum, long-term measurement, spectrogram (spectrogram requires R&S®RTP-K37 option)
Horizontal divisions	10
Vertical divisions	10
Display interface configuration	display area can be split up into separate diagram areas by dragging and dropping signal icons; each diagram area can hold any number of signals; diagram areas may be stacked on top of each other and later accessed via the dynamic tab menu
Signal icon	each active waveform is represented by a separate signal icon on the signal bar; the signal icon displays individual vertical and acquisition settings; a waveform can be minimized to signal icon to appears as a realtime preview in miniature; measurement results may also be minimized to a signal icon

Toolbar	quick access to 28 important tools; directly set most common parameters in a simple menu and access to more detailed parameters in main menu; user-defined selection of tools in toolbar
Upper menu	displays trigger, horizontal and acquisition settings; quick access to settings
Main menu	provides access to all instrument settings in compact menu
Axis label	X-axis ticks and Y-axis ticks labeled with tick value and physical unit
Diagram label	diagrams may be individually labeled with a descriptive user-defined name
Diagram layout	grid, crosshair, axis labels and diagram label may be switched on and off separately
Persistence	50 ms to 50 s, or infinite
Zoom	user-defined zoom window provides vertical and horizontal zoom; each diagram area supports multiple zoom windows; touchscreen interface simplifies resize and drag operations on zoom window
Signal colors	predefined or user-defined color tables for persistence display

Input and output

Front		
Channel inputs		BNC-compatible, for details see Vertical system
	probe interface	auto-detection of passive probes, Rohde & Schwarz active probe interface
External trigger input		BNC, for details see Trigger system
	probe interface	auto-detection of passive probes, Rohde & Schwarz active probe interface
Probe compensation output	signal shape	rectangle, V_{low} = 0 V, V_{high} = 1 V amplitude 1 V (V_{pp}) ± 5 %
	frequency	1 kHz ± 1 %
	impedance	50 Ω (nom.)
Ground jack		4 mm, connected to ground
USB interface		2 ports, type A plug, version 3.1 gen 1
Option slots		2
Rear		
Trigger out		BNC, for details see Trigger system
USB interface		2 ports, type A plug and 1 port, type B plug, version 3.1 gen 1
LAN interface		RJ-45 connector, supports 10/100/1000BASE-T
External monitor interface		HDMI 2.0 and DisplayPort++ 1.3, output of oscilloscope display or extended desktop display
GPIB interface	function	interface in line with IEC 625-2 (IEEE 488.2)
	command set	SCPI 1999.0
	connector	IEEE-488 24-pin Amphenol female
	interface functions	SH1, AH1, T6, L4, SR1, RL1, PP1, DC1, DT1, C0
External reference input	connector	BNC female
	impedance	50 Ω (nom.)
	input frequency range	1 MHz to 20 MHz in steps of 1 MHz
	sensitivity	≥ 0 dBm into 50 Ω
Reference output 10 MHz	connector	BNC female
	impedance	50 Ω (nom.)
	level	> 7 dBm
Auxiliary output		SMA connector, for future use
Digital data interface 40G		QSFP+ connector, for future use
Option slots		2
Security slot		for standard Kensington style lock

General data

Display	type	13.3" LC TFT color display with capacitive touchscreen
	resolution	1920 × 1080 pixel (Full HD)
Operating system		Windows 10 64-bit
Hard disk drive		≥ 256 Gbyte removeable SSD

Temperature	operating	+5 °C to +45 °C
	non-operating	–40 °C to +70 °C, in line with MIL-PRF-28800F section 4.5.5.1.1.1 class 3
Humidity		+25° C/+40 °C at 85 % rel. humidity cyclic, in line with IEC 60068-2-30
		+30 °C/+40 °C/+45 °C at 95 %/75 %/45 %, in line with MIL-PRF-28800F section 4.5.5.1.1.2 class 3 for operation
Altitude	operating	up to 3000 m/9 843 ft above sea level
	non-operating	up to 4600 m/15 093 ft above sea level
Vibration	operating	sinusoidal: 5 Hz to 150 Hz, max. 1.8 g at 55 Hz, 0.5 g from 55 Hz to 150 Hz, in line with EN 60068-2-6
		random: 8 Hz to 500 Hz, acceleration 1.2 g (RMS), in line with EN 60068-2-64
	non-operating	shock: 40 g shock spectrum, in line with MIL-STD-810E, method no. 516.4, procedure I

EMC		
RF emission		in line with CISPR 11/EN 55011 group 1 class A (for a shielded test setup); the instrument complies with the emission requirements stipulated by EN 55011, EN 61326-1 and EN 61326-2-1 class A, making the instrument suitable for use in industrial environments
Immunity		in line with IEC/EN 61326-1 table 2, immunity test requirements for industrial environment [7]

Certifications		VDE, $_{C}$CSA$_{US}$, CE, KC, UKCA, RCM

Calibration interval		1 year

Power supply		
AC supply		100 V to 240 V at 50 Hz to 60 Hz, 100 V to 130 V at 400 Hz, max. 13 A to 4.7 A, in line with MIL-PRF-28800F section 3.5
Power consumption		max. 1000 W
Safety		in line with IEC 61010-1, EN 61010-1, CAN/CSA-C22.2 No. 61010-1, UL 61010-1

Mechanical data		
Dimensions (W × H × D)	with R&S®RTP-B20 handles	463 mm × 285 mm × 349 mm (18.23 in × 11.22 in × 13.74 in)
	with shock protection	441 mm × 285 mm × 316 mm (17.36 in × 11.22 in × 12.44 in)
Weight	without options, nominal	18.0 kg (39.68 lb)

[7] Test criterion is displayed noise level within ±1 div for input sensitivity of 5 mV/div.

Options

R&S®RTP-B1 mixed signal option

Mixed signal option, additional 16 logic channels

Vertical system

Input channels		16 logic channels (D0 to D15)
Arrangement of input channels		arranged in two logic probes with 8 channels each, assignment of the logic probes to the channels (D0 to D7 or D8 to D15) is displayed on the probe
DC input resistance	at probe tips	100 kΩ ± 2 % (meas.)
Input capacitance		4 pF (meas.)
Maximum input frequency	signal with minimum input voltage swing and hysteresis setting: normal	400 MHz (meas.)
Maximum input voltage		±40 V (V_p)
Minimum input voltage swing		500 mV (V_{pp}) (meas.)
Input dynamic range		±8.5 V (meas.)
Resolution		1 bit
Threshold groups		D0 to D3, D4 to D7, D8 to D11 and D12 to D15
Threshold level	range	±8 V in steps of 25 mV
	predefined	CMOS 5.0 V, CMOS 3.3 V, CMOS 2.5 V, TTL, ECL, PECL, LVPECL
Threshold accuracy	threshold setting between ±4 V	±(100 mV + 3 % of threshold setting) (meas.)
Comparator hysteresis		normal, robust, maximum

Horizontal system

Channel deskew	range for each channel	±200 ns in steps of 200 ps
Channel-to-channel skew		< 500 ps (meas.)

Acquisition system

Sampling rate	max.	5 Gsample/s on each channel
Realtime waveform acquisition rate	max.	> 200 000 waveforms/s
Memory depth	at max. sampling rates	200 Mpoints for every channel
	at lower sampling rates	100 Mpoints for every channel
Decimation		pulses lost due to decimation are displayed
Minimum detectable pulse width		500 ps (meas.)

Trigger system

Holdoff range	time	100 ns to 10 s, fixed and random
	events	1 event to 2 000 000 000 events

Trigger modes		
Edge	triggers on specified slope (positive, negative or either) in the source signal	
	sources	any channel from D0 to D15 or any logical combination of D0 to D15
Width	triggers on positive or negative pulse of specified width in the source signal; width can be shorter, longer, equal, inside or outside the interval	
	sources	any channel from D0 to D15 or any logical combination of D0 to D15
	pulse width	200 ps to 10 s
Timeout	triggers when the source signal stays high, low or unchanged for a specified period of time	
	sources	any channel from D0 to D15 or any logical combination of D0 to D15
	timeout	200 ps to 10 s

Data2clock	triggers on setup time and hold time violations between a clock signal and a data signal; monitored time interval with a max. width of 200 ns and a position of max. ±1 µs relative to the clock edge	
	data signal	any subset of channels from D0 to D15 or any user-defined bus signal
	clock signal	any channel from D0 to D15
Pattern	triggers when the source goes true or stays true for a period of time shorter, longer, equal, inside or outside a specified range	
	sources	any logical combination of D0 to D15 or any user-defined bus signal
	pulse width	200 ps to 10 s
State	triggers on the slope (positive, negative or either) of the clock signal when data signal matches a user-defined logical state	
	data signal	any logical combination of D0 to D15 or any user-defined bus signal
	clock signal	any channel from D0 to D15
Serial pattern	triggers on a serial data pattern of up to 32 bit; pattern bits may be high (H), low (L) or don't care (X); clock edge slope may be positive, negative or either	
	data signal	any channel from D0 to D15 or any logical combination of D15 to D15
	clock signal	any channel from D0 to D15
	max. data rate	1 Gbps
Serial bus trigger	optional	dedicated software options
	sources	any channel from D0 to D15

Waveform measurements

General features		measurement panels, gate, statistics, long-term analysis and limit check; see features of the base unit
Measurement sources		all channels from D0 to D15 or any logical combination of D0 to D15
Automatic measurements		positive pulse width, negative pulse width, period, frequency, burst width, delay, phase, positive duty cycle, negative duty cycle, positive pulse count, negative pulse count, rising edge count, falling edge count
Additional cursor function		display of decoded bus value at the cursor position

Waveform math

Function		any logical combination of D0 to D15

Search and mark functions

The search function will be available in a future software release.

Display characteristics

Display of logical channels		selectable size and position on screen, diagram configuration by dragging and dropping signal icons
Bus decode	number of bus signals	4
	bus types	unclocked and clocked
	display types	decoded bus, logical signal, bus + logical signal, amplitude signal, amplitude + logical signal, tabulated list (decoded time interval selected with cursors)
	position and size	size and position on screen selectable
	data format of decoded bus	hex, unsigned integer, signed integer, fractional, binary
	data format of amplitude signal	unsigned integer, signed integer, fractional, binary offset
Channel activity display		independent of the oscilloscope acquisition, the state (stays low, stays high or toggles) of the channels from D0 to D15 is displayed in the signal icon

R&S®RTP-B6 arbitrary waveform generator

Arbitrary function/waveform generator, 2 analog channels, 8-bit pattern generator

Analog channels

General		
Output channel		2 channels
Vertical resolution		14 bit
Operating modes		function generator, arbitrary waveform generator, modulation, frequency sweep

Function generator	output of predefined waveforms	
Sample rate		500 Msample/s
Waveforms	sine, square, ramp, DC, noise, pulse, cardinal sine (sinc), cardiac, Gaussian pulse, Lorentz, exponential rise, exponential fall	
Sine	frequency range	1 mHz to 100 MHz in steps of 1 mHz
	amplitude flatness (relative to 1 kHz)	
	f ≤ 100 kHz	≤ ±0.1 dB
	100 kHz < f ≤ 60 MHz	≤ ±0.3 dB
	60 MHz < f ≤ 100 MHz	≤ ±0.5 dB
	total harmonic distortion (THD at 1 V (V_{pp}) into 50 Ω)	
	f ≤ 100 kHz	≤ –70 dBc (= THD ≤ 0.032 %)
	100 kHz < f ≤ 15 MHz	≤ –55 dBc
	15 MHz < f ≤ 35 MHz	≤ –40 dBc
	35 MHz < f ≤ 100 MHz	≤ –30 dBc
	nonharmonic spurious (1 V (V_{pp}) into 50 Ω)	–65 dBc (meas.)
	phase noise (meas.)	
	f ≤ 25 MHz	≤ –105 dBc (1 Hz) at 1 kHz offset, ≤ –115 dBc (1 Hz) at 10 kHz offset, ≤ –125 dBc (1 Hz) at 100 kHz offset
	25 MHz < f ≤ 100 MHz	≤ –105 dBc (1 Hz) at 1 kHz offset, ≤ –110 dBc (1 Hz) at 10 kHz offset, ≤ –115 dBc (1 Hz) at 100 kHz offset
Square, pulse	frequency range	1 mHz to 30 MHz in steps of 1 mHz
	duty cycle (if pulse width limit is not exceeded)	0.01 % to 99.99 % in steps of 0.01 %
	duty cycle accuracy (meas.)	
	50 % duty cycle	≤ 0.001 % or ≤ 100 % · 150 ps · f whichever is larger f = frequency of square/ pulse signal
	any duty cycle	≤ 0.5 %
	pulse width	≥ 16.5 ns in steps of 0.1 ns
	rise/fall time	
	f ≤ 10 Hz	90 µs (meas.)
	10 Hz < f ≤ 30 MHz	9 ns (meas.)
	overshoot	≤ 2 %
	jitter (cycle-to-cycle)	≤ 40 ps (RMS) (meas.)
Ramp (triangle, sawtooth)	frequency range	1 mHz to 1 MHz in steps of 1 mHz
	linearity	≤ 0.1 % (meas.)
	variable symmetry	0 % to 100 % in steps of 0.1 %
DC	level range	
	into 50 Ω	± [3 V – (noise amplitude [V_{pp}] / 2)]
	into open circuit	± [6 V – (noise amplitude [V_{pp}] / 2)]
Noise	amplitude	
	DC	0 V to 6 V (V_{pp}) (into 50 Ω), 0 V to 12 V (V_{pp}) (into open circuit), 4 digits resolution
	all other waveforms	0 % to 100 % of AC signal amplitude, 1 % resolution
	bandwidth	≥ 100 MHz
Cardinal sine (sinc)	frequency range	1 mHz to 5 MHz
Cardiac	frequency range	1 mHz to 1 MHz
Gauss (Gaussian pulse)	frequency range	1 mHz to 25 MHz
Lorentz	frequency range	1 mHz to 10 MHz
Exponential rise/fall	frequency range	1 mHz to 1 MHz

Arbitrary waveform generator	output of user-defined waveforms	
Waveform length		1 point to 40 Mpoints on each channel
Sample rate		1 sample/s to 250 Msample/s
Filter bandwidth		100 MHz

Modulation		
Sample rate		500 Msample/s
Modulation types		amplitude modulation (AM), frequency modulation (FM), frequency-shift key modulation (FSK), pulse width modulation (PWM)
Carrier waveform	AM, FM, FSK	sine
	PWM	square/pulse
AM	carrier frequency	1 mHz to 100 MHz
	modulation signals	sine, square, ramp (triangle, sawtooth)
	modulation frequency	1 mHz to 1 MHz
	modulation depth	0 % to 100 % in steps of 0.1 %
FM	carrier frequency	1 mHz to 100 MHz
	modulation signals	sine, square, ramp (triangle, sawtooth)
	modulation frequency	1 mHz to 1 MHz
	frequency deviation	1 mHz to 10 MHz
FSK	modulation signal	50 % duty cycle square wave
	range of frequency 1, frequency 2	1 mHz to 100 MHz
	hop rate	1 mHz to 1 MHz
PWM	carrier frequency	1 mHz to 30 MHz
	modulation signals	sine, square, ramp (triangle, sawtooth)
	modulation frequency	1 mHz to 1 MHz
	modulation depth	0 % to 99.99 % of the duty cycle, 0.01 % resolution

Frequency sweep	output of a sinusoidal waveform with the frequency changing linearly between the start frequency and the stop frequency within the sweep time	
	sample rate	500 Msample/s
	waveform	sine
	frequency range	1 mHz to 100 MHz
	direction	up (start frequency < stop frequency)
		down (start frequency > stop frequency)
	sweep time	1 ms to 500 s

Two-channel operation	operating modes	independent channels, coupled parameters, differential
	parameter coupling	none, frequency and/or amplitude
	relative phase	–180° to 180° in steps of 0.1°
	channel-to-channel skew	≤ 200 ps (meas.)
	channel-to-channel isolation (each channel with same output amplitude)	
	f ≤ 10 MHz	≥ 60 dB (meas.)
	10 MHz < f ≤ 100 MHz	≥ 40 dB (meas.)

Outputs		
Connectors		BNC female on the rear panel
Function		on, off, inverted
Output impedance		50 Ω (nom.)
Overload protection		a short-circuit to ground is tolerated indefinitely, automatic shutoff in case of voltages ≥ +7 V or ≤ –7 V (meas.), automatic shutoff in case of overcurrent, max. –20 V to +20 V without damage (meas.), ESD protection

Amplitude range [8]	sine, square, ramp, pulse, exponential rise, exponential fall	
	into 50 Ω	10 mV to 6 V (V_{pp}) (frequency ≤ 50 MHz), 10 mV to 4 V (V_{pp}) (frequency > 50 MHz)
	into open circuit	20 mV to 12 V (V_{pp}) (frequency ≤ 50 MHz), 20 mV to 8 V (V_{pp}) (frequency > 50 MHz)
	cardinal sine (sinc), cardiac	
	into 50 Ω	10 mV to 3 V (V_{pp})
	into open circuit	20 mV to 6 V (V_{pp})
	Gauss (Gaussian pulse), Lorentz	
	into 50 Ω	10 mV to 2.5 V (V_{pp})
	into open circuit	20 mV to 5 V (V_{pp})
	arbitrary waveforms	
	into 50 Ω	10 mV to 6 V (V_{pp}) (sample rate ≤ 125 Msample/s), 10 mV to 4 V (V_{pp}) (sample rate > 125 Msample/s)
	into open circuit	20 mV to 12 V (V_{pp}) (sample rate ≤ 125 Msample/s), 20 mV to 8 V (V_{pp}) (sample rate > 125 Msample/s)
	resolution	1 mV
	accuracy	± [1% of control + 1 mV (V_{pp})] at 1 kHz
DC offset range	sine, square, ramp, pulse, exponential rise, exponential fall	
	into 50 Ω	± [3 V – (amplitude [V (V_{pp})] / 2)]
	into open circuit	± [6 V – (amplitude [V (V_{pp})] / 2)]
	cardinal sine (sinc), cardiac, Gauss (Gaussian pulse), Lorentz	
	into 50 Ω	±0.5 V
	into open circuit	±1 V
	resolution	1 mV
	accuracy	± (2 % of control + 2 mV)
Frequency accuracy		| Δf | ≤ [(timebase accuracy) × (nominal frequency) + 1 µHz] (timebase accuracy: see Horizontal system)

8-bit pattern generator

Function		output of user-defined patterns
Output channels		8 channels, coupled w.r.t. pattern length and data output rate
Pattern length		1 bit to 40 Mbit on each channel
Bit rate		1 bit/s to 40 Mbit/s

Outputs		
Connector		16-pin double row connector, 2.54 mm pitch, located on an adapter board, which is connected via a removable ribbon cable to the R&S®RTP-B6
Output impedance		330 Ω (nom.)
Overload protection	reverse input voltage without damage	–0.5 V to +6.5 V (meas.), ESD protection
Amplitude	low level output voltage (I = 100 µA)	
	output voltage	0 V + 0.15 V/– 0.02 V
	accuracy	≤ 0.15 V (meas.)
	high level output voltage	
	setting range	1.2 V to 5.0 V in steps of 0.1 V
	accuracy	≤ 0.05 V
Rise/fall time		8 ns (meas.)
Overshoot		≤ 5 % (meas.)

[8] Amplitude is the sum of the AC amplitude and the noise amplitude.

R&S®RTP-B7 16 GHz differential pulse source

16 GHz differential pulse source with reference output

Output [9]

Output pulse		two complementary negative going square wave pulse train signals, single-ended or differential operation, fast transition on rising and falling edge, adjustable amplitude and timing parameters, free-running or phase-locked to base unit
Outputs	single-ended operation	single-ended output (OutP)
		single-ended reference output (RefP)
	differential operation	differential output (OutP, OutN)
		differential reference output (RefP, RefN)
Output connectors		SMA female connectors
Reverse DC voltage		0 V
Output impedance	single-ended outputs	50 Ω (nom.)
	both differential pairs	100 Ω (nom.)
Return loss	≤ 10 GHz	> 15 dB (meas.)
	≤ 20 GHz	> 12 dB (meas.)

DC characteristics [9]

Output high level		0 V ± 10 mV
Output low level setting range		–200 mV to –50 mV in steps of 10 mV
Output low level error	OutP	±2 % of setting ±15 mV
Output low level imbalance	between OutP and RefP, OutN, RefN	±1 dB (meas.)

Time domain characteristics [9]

Transition time	10 % to 90 %, rising and falling edge, calculated from 0.36/bandwidth	
	output low level: –120 mV to –50 mV	20 ps
	output low level: –200 mV to –130 mV	22 ps
Step response aberrations	for the first 100 ps after step transition	±10 % (meas.)
	for the first 1 ns after step transition	±4 % (meas.)
	until 100 ps before following step transition	±2 % (meas.)
Repetition rate	low frequency mode	5/10/20/50/100/200/500 Hz to 1 MHz
	high frequency mode, phase-locked to base unit	5/10/25/50/100/250 MHz
	high frequency mode, free-running	5/10/25/50 MHz
Positive duty cycle	measured at 50 % of transition	
	low frequency mode	10 % to 90 % in steps of 10 %
	high frequency mode	50 %
Duty cycle error	measured at 50 % of transition, at OutP and RefP outputs	
	low frequency mode	±2 % (meas.)
	high frequency mode	±0.1 % (meas.)
Skew	measured at 50 % of transition, between OutP and OutN output	< 0.5 ps (meas.)
Clock accuracy	free-running	±100 ppm (meas.)
	phase-locked to base unit	see Timebase accuracy of base unit

Frequency domain characteristics [9]

Analog bandwidth (–3 dB)	output low level: –120 mV to –50 mV	> 18 GHz (meas.)
	output low level: –200 mV to –130 mV	> 16.5 GHz (meas.)
Spectral magnitude error to ideal step spectrum	≤ 5 GHz	+0.5 dB to –1 dB (meas.)
	≤ 12 GHz	+0.5 dB to –2 dB (meas.)
	≤ analog bandwidth	+0.0 dB to –3 dB (meas.)

[9] All four outputs terminated with 50 Ω; all parameters are measured at all four single-ended outputs, unless noted.

General

Accessories	The R&S®RTP-B7 contains an accessory bag with 2 SMA cables, 4 SMA terminations, 2 SMA(f) to SMA(f) adapters, 2 SMA shorts and 1 ESD wrist strap with grounding cord.

R&S®RTP-K1 I²C/SPI serial triggering and decoding

I²C triggering and decoding		
Protocol configuration	bit rate	auto-detected
	auto threshold setup	assisted threshold configuration for I²C triggering and decoding
	device list	associate frame address with symbolic ID
Trigger	source (clock and data)	any input channel or logical channel
	bit rate	up to 6.5 Mbps
	trigger event setup	start, stop, restart, missing ACK, address, data, address + data
	address setup	7 bit or 10 bit address (value in hex, decimal, octal or binary); ACK, NACK or either; read, write or either; R/W bit included in address value or apart; condition =, ≠, ≥, ≤, in range, out of range
	data setup	data pattern up to 8 byte (hex, decimal, octal or binary); condition =, ≠, ≥, ≤, in range, out of range; offset within frame in range from 0 byte to 4095 byte
Decode	source (clock and data)	any input channel, math waveform, reference waveform, logical channel
	display type	decoded bus, logical signal, bus + logical signal, tabulated list, decode layers
	color coding	frame, start/restart, address, R/W bit, data, ACK/NACK, stop, error
	address and data format	hex, decimal, octal, binary, ASCII; symbolic names for user-defined subset of addresses
	decode layer	off, edges, bit
Search	search event setup	combination of start, stop, restart, missing ACK, address, data, address + data
	event settings	same as trigger event settings

SPI triggering and decoding		
Protocol configuration	type	2-wire, 3-wire and 4-wire SPI
	bit rate	auto-detected
	bit order	LSB first, MSB first
	word size	4 bit to 32 bit
	frame condition	SS, timeout
	polarity (MOSI, MISO, SS, CLK)	active high, active low
	phase (CLK)	first edge, second edge
	auto threshold setup	assisted threshold configuration for SPI triggering and decoding
Trigger	source (MOSI, MISO, SS, CLK)	any input channel or logical channel
	bit rate	up to 50 Mbps
	trigger event setup	start of frame, MOSI, MISO, MOSI + MISO
	data setup	data pattern up to 256 bit (hex or binary); condition =, ≠; offset within frame in range from 0 bit to 32767 bit
Decode	source (MOSI, MISO, SS, CLK)	any input channel, math waveform, reference waveform, logical channel
	display type	decoded bus, logical signal, bus + logical signal, tabulated list, decode layers
	color coding	frame, word, error
	data format	hex, decimal, octal, binary, ASCII
	decode layer	edges, bit, words
Search	search event setup	start of frame, MOSI, MISO, MOSI + MISO
	event settings	same as trigger event settings

R&S®RTP-K2 UART/RS-232/RS-422/RS-485 serial triggering and decoding

Protocol configuration	bit rate	300 bps to 20 Mbps
	signal polarity	idle low, idle high
	number of bits	5 bit to 9 bit
	bit order	LSB first, MSB first
	parity	odd, even, mark, space, none
	stop bit	1, 1.5 or 2 bit periods
	end of packet	word, timeout, none
	auto threshold setup	assisted threshold configuration for UART triggering and decoding
Trigger	source (TX and RX)	any input channel or logical channel
	trigger event setup	start bit, packet start, data, parity error, break condition
	data setup	data pattern up to 256 bit (hex, decimal, octal, binary or ASCII); condition =, ≠; offset within packet in range 0 bit to 32767 bit
Decode	source (TX and RX)	any input channel, math waveform, reference waveform, logical channel
	display type	decoded bus, logical signal, bus + logical signal, tabulated list
	color coding	packet, data payload, start error, parity error, stop error
	data format	hex, decimal, octal, binary, ASCII

R&S®RTP-K3 CAN/LIN serial triggering and decoding

CAN triggering and decoding		
Protocol configuration	signal type	CAN_H, CAN_L
	bit rate	100 bps to 1 Mbps
	sampling point	5 % to 95 % within bit period
	device list	associate frame identifier with symbolic ID, load DBC file content
	auto threshold setup	assisted threshold configuration for CAN triggering and decoding
Trigger	source	any input channel or logical channel
	trigger event setup	start of frame, frame type, identifier, identifier + data, symbolic, error condition (any combination of CRC error, bit stuffing error, form error and ACK error)
	identifier setup	frame type (data, remote or both), identifier type (standard or extended); condition =, ≠, ≥, ≤, in range, out of range
	data setup	data pattern up to 8 byte (hex, decimal, octal or binary); big-endian or little-endian; condition =, ≠, ≥, ≤, in range, out of range
	symbolic setup	message name, signal name; numeric signal condition =, ≠, ≥, ≤, in range, out of range; enumerated signal condition =, ≠, ≥, ≤
Decode	source	any input channel, math waveform, reference waveform, logical channel
	display type	decoded bus, logical signal, bus + logical signal, tabulated list
	color coding	start of frame, identifier, DLC, data payload, CRC, end of frame, error frame, overload frame, CRC error, bit stuffing error
	data format	hex, decimal, octal, binary, ASCII, symbolic

Search	source	any input channel or logical channel
	search event setup	combination of start of frame, frame type, identifier, identifier + data, error condition (any combination of CRC error, bit stuffing error, form error and ACK error) or only symbolic
	event settings	same as trigger event settings

LIN triggering and decoding		
Protocol configuration	version	1.3, 2.x or SAE J602; mixed traffic is supported
	bit rate	standard bit rate (1.2/2.4/4.8/9.6/10.417/ 19.2 kbps) or user-defined bit rate in range from 1 kbps to 20 kbps
	device list	associate frame identifier with symbolic ID, data length and protocol version
	auto threshold setup	assisted threshold configuration for LIN triggering and decoding
Trigger	source	any input channel
	trigger event setup	start of frame (sync break), identifier, identifier + data, wake-up frame, error condition (any combination of checksum error, parity error and sync field error)
	identifier setup	range from 0d to 63d; select condition =, ≠, ≥, ≤, in range, out of range for trigger “identifier”; select single identifier and condition = for trigger “identifier + data”
	data setup	data pattern up to 8 byte (hex, decimal, octal or binary); condition =, ≠, ≥, ≤, in range, out of range
Decode	source (TX and RX)	any input channel, math waveform, reference waveform
	display type	decoded bus, logical signal, bus + logical signal, tabulated list
	color coding	frame, frame identifier, data payload, checksum, error condition
	data format	hex, decimal, octal, binary, ASCII
Search	search event setup	combination of start of frame (sync break), identifier, identifier + data, wake-up frame, error condition (any combination of checksum error, parity error and sync field error)
	event settings	same as trigger event settings

R&S®RTP-K6 MIL-STD-1553 serial triggering and decoding

Protocol configuration	signal type	single-ended
	bit rate	standard bit rate (1 Mbit/s)
	polarity	normal, inverted
	device list	associate frame identifier with symbolic ID
	auto threshold setup	assisted threshold configuration
	timing	min. gap (2 µs to 262 µs) or off; max. response (2 µs to 262 µs) or off
Trigger	trigger event setup	sync, word, data word, command/status word, command word, status word, error condition
	sync and word setup	all words, command/status word, data word
	data word setup	RTA (condition =, ≠, ≥, ≤, in range, out of range); data pattern (condition =, ≠, ≥, ≤, in range, out of range); payload data index (=, <, >, ≥, ≤, range); max. length of data pattern is 4 byte
	command/status word setup	RTA (condition =, ≠, ≥, ≤, in range, out of range); 11 bit pattern (condition =, ≠, ≥, ≤, in range, out of range)
	command word setup	RTA (condition =, ≠, ≥, ≤, in range, out of range); subaddress/mode (condition =, ≠, ≥, ≤, in range, out of range); data word count/mode count (condition =, ≠, ≥, ≤, in range, out of range); direction (T/R)
	status word	RTA (condition =, ≠, ≥, ≤, in range, out of range); status flags (message error, instrumentation, service request, broadcast command, busy, subsystem flag, dynamic bus control, terminal flag)
	error condition	any combination of sync error, Manchester error, parity error, timing error (see protocol configuration)
Decode	source	any analog input channel, math waveform, reference waveform
	display type	decoded bus, logical signal, bus + logical signal, tabulated list
	color coding	frame (word), sync, RTA, status bit field, parity, data field, error condition
	data format	hex, octal, binary, ASCII, signed, unsigned
Search	search event setup	sync, word, data word, command/status word, command word, status word, error condition
	event settings	same as trigger event settings

R&S®RTP-K7 ARINC 429 serial triggering and decoding

Protocol configuration	signal type	single-ended
	bit rate	high (100 kbit/s)
		low (12 kbit/s to 14.5 kbit/s)
	polarity	A leg, B leg
	device list	associate frame identifier with symbolic ID
	auto threshold setup	assisted threshold configuration
	timing	min. gap (0 bit to 100 bit) or off; max. gap (0 bit to 1000 bit) or off
Trigger	trigger event setup	word start, word stop, label + data, error condition
	label + data setup	label (condition =, ≠, ≥, ≤, in range, out of range); data (condition =, ≠, ≥, ≤, in range, out of range); SDI/SSM
	error condition	any combination of coding error, parity error, timing error (see protocol configuration)
Decode	source	any analog input channel, math waveform, reference waveform
	display type	decoded bus, logical signal, bus + logical signal, tabulated list
	color coding	frame (word), label, SDI, data, SSM, parity, error condition
	data format	hex, octal, binary, ASCII, signed, unsigned
Search	search event setup	word start, word stop, label + data, error condition
	event settings	same as trigger event settings

R&S®RTP-K8 Ethernet (10BASE-T/100BASE-TX) serial triggering and decoding

Protocol configuration	signal type	one differential channel
	bit rate	auto-detected
	auto threshold setup	assisted threshold configuration
	full autoset	adjust horizontal and vertical resolution and perform auto threshold
	source (SDATA)	analog and math channels
	variants	10BASE-T, 100BASE-TX
Trigger	frame start	trigger at start of any MAC frame
	pattern	fast trigger for 10BASE-T MAC frames, 32 byte, index 0 to 65535
	frame	advanced trigger configuration for MAC frames only; 48 bit destination address, 48 bit source address, 16 bit length/type, 32 bit frame check; conditions =, ≠, <, ≤, >, ≥, in range, out of range
	error	preamble error, length error, CRC error
Decode	display type	decoded bus, logical signal, bus + logical signal, tabulated list, details, decode layers
	color coding	preamble, frame, destination address, source address, data
	data format	hex, octal, binary, signed, unsigned
	decode layer	edges, binary
	result export	export of all result data into CSV, XML, HTML and PY file formats
Search	search event setup	frame, error
	event settings	same as trigger event settings

R&S®RTP-K9 CAN-FD serial triggering and decoding

Protocol configuration	signal type	CAN_H, CAN_L
	standard	ISO, non-ISO (Bosch)
	bit rate	
	arbitration rate	10 kbps to 1 Mbps
	data rate	10 kbps to 15 Mbps
	sampling point	5 % to 95 % within bit period; independent settings for arbitration phase and data phase
	device list	associate frame identifier with symbolic ID, load DBC file content
	auto threshold setup	assisted threshold configuration
Trigger	source	any input channel or logical channel
	trigger event setup	start of frame, frame type, identifier, identifier + data, symbolic, error condition (any combination of CRC error, bit stuffing error, form error and ACK error)
	identifier setup	frame type (data, remote or both), identifier type (standard or extended); condition =, ≠, ≥, ≤, in range, out of range
	FD bit	FDF, BRS and ESI (0, 1, X)
	data setup	data pattern up to 8 byte in the complete data range (hex, decimal, octal or binary); condition =, ≠, ≥, ≤, in range, out of range
	symbolic setup	message name, signal name; numeric signal condition =, ≠, ≥, ≤, in range, out of range; enumerated signal condition =, ≠, ≥, ≤
Decode	source	any input channel, math waveform, reference waveform, logical channel
	display type	decoded bus, logical signal, bus + logical signal, tabulated list
	color coding	start of frame, identifier, FD bit, DLC, data payload, CRC, end of frame, error frame, overload frame, CRC error, bit stuffing error
	data format	hex, decimal, octal, binary, ASCII, symbolic
	supported data length	64
Search	source	any input channel or logical channel
	search event setup	combination of start of frame, frame type, identifier, identifier + data, error condition (any combination of CRC error, bit stuffing error, form error and ACK error) or only symbolic
	event settings	same as trigger event settings

R&S®RTP-K11 I/Q software interface

General	function		mixing, filtering, decimation and recording of RF or baseband signals as I/Q samples	
	input signals		four real RF signals or two complex I/Q signals or two real RF signals and one complex I/Q signal	
	mixer frequency		between 100 Hz and 20 GHz (or mixer deactivated)	
	sampling rate of recorded I/Q samples		between 1 ksample/s and 20 Gsample/s user-selectable	
	digital filter bandwidth (flat frequency response)		4 % to 80 % of sampling rate	
	recording length		max. 40 Mpoints with four input signals [10]	
Trigger	mode		auto or normal	
	operation		triggers on acquired signal after A/D conversion serial bus and MSO trigger not available	
Display			magnitude of the downconverted signals	
Amplitude flatness with RF signal input (meas.)	R&S®RTP044B	max. used center frequency	with I/Q bandwidth 100 MHz	with I/Q bandwidth 500 MHz
		≤ 100 MHz	±0.10 dB	
		≤ 500 MHz	±0.2 dB	±0.2 dB
		≤ 1 GHz	±0.2 dB	±0.3 dB
		≤ 2 GHz	±0.2 dB	±0.3 dB
		≤ 4 GHz	±0.4dB	±1.8 dB
	R&S®RTP064B	max. used center frequency	with I/Q bandwidth 100 MHz	with I/Q bandwidth 500 MHz
		≤ 100 MHz	±0.10 dB	
		≤ 500 MHz	±0.2 dB	±0.2 dB
		≤ 1 GHz	±0.2 dB	±0.3 dB
		≤ 2 GHz	±0.2 dB	±0.3 dB
		≤ 4 GHz	±0.3 dB	±0.3 dB
		≤ 6 GHz	±0.5 dB	±2.0 dB
	R&S®RTP084B	max. used center frequency	with I/Q bandwidth 100 MHz	with I/Q bandwidth 500 MHz
		≤ 100 MHz	±0.10 dB	
		≤ 500 MHz	±0.2 dB	±0.2 dB
		≤ 1 GHz	±0.2 dB	±0.3 dB
		≤ 4 GHz	±0.3 dB	±0.3 dB
		≤ 8 GHz	±0.5 dB	±2.0 dB
	R&S®RTP134B	max. used center frequency	with I/Q bandwidth 100 MHz	with I/Q bandwidth 500 MHz
		≤ 100 MHz	±0.10 dB	
		≤ 500 MHz	±0.2 dB	±0.2 dB
		≤ 1 GHz	±0.2 dB	±0.3 dB
		≤ 4 GHz	±0.3 dB	±0.3 dB
		≤ 8 GHz	±0.5 dB	±2.0 dB
	R&S®RTP164B	max. used center frequency	with I/Q bandwidth 100 MHz	with I/Q bandwidth 500 MHz
		≤ 100 MHz	±0.10 dB	
		≤ 500 MHz	±0.2 dB	±0.2 dB
		≤ 1 GHz	±0.2 dB	±0.3 dB
		≤ 4 GHz	±0.3 dB	±0.3 dB
		≤ 8 GHz	±0.5 dB	±2.0 dB

[10] Maximum recording length of 25 Msample for sampling rates of recorded I/Q samples: 250 Msample/s to 400 Msample/s.

R&S®RTP-K12 jitter analysis

General description	The R&S®RTP-K12 jitter analysis option extends the functionality of the standard R&S®RTP firmware with a suite of measurement, analysis and visualization tools for signal integrity analysis and jitter characterization.	
Waveform measurements	category	jitter
	measurement functions	cycle-to-cycle jitter, N-cycle jitter, cycle-to-cycle width, cycle-to-cycle duty cycle, time-interval error, data rate, unit interval, skew delay, skew phase; the standard time measurements period, frequency and setup/hold are also available in the jitter category for convenience
	track	measurement results displayed as continuous trace that is time-correlated to the measurement source; applicable to time measurements from categories “jitter” and “amplitude and time”; track trace may be used as source for cursor measurements, automatic measurements, math waveforms and reference waveforms
Waveform math	FFT on track	FFT spectrum of the track trace of measurement results
	CDR transform	recovers clock timing from source waveform with software CDR and generates synthetic clock waveform that is time-correlated to source
Software clock data recovery (CDR)	number of CDR instances	up to 2; independently configurable
	algorithm	phase-locked loop (PLL), constant frequency
	configuration	nominal bit rate, PLL order (first or second), PLL loop bandwidth, PLL damping factor, initial phase alignment, result selection during initial synchronization
Mask testing with eye mask assistant	primary mask shape	
	type	diamond, square, hexagon, octagon
	dimensions	main and secondary height, main and secondary width, depending on selected shape
	position	vertical offset, horizontal offset
	secondary mask shapes	
	locations	any combination of left, right, top, bottom
	position	horizontal and vertical offset with respect to center of primary mask shape

R&S®RTP-K19 zone trigger

General description	The R&S®RTP-K19 zone trigger enables the triggering on user-defined zones drawn on the display.	
Source		acquired waveforms (input channels), math waveforms
Zone definition	number of zones	up to 8
	shapes	rectangles, polygones
	types	must intersect, must not intersect
	combination of zones	logical combination of zones of multiple sources using Boolean expressions
Trigger compatibility		compatible with the trigger modes edge, glitch, width, runt, window, timeout, interval, slew rate, data2clock, pattern, state, serial pattern, trigger qualification, and sequence trigger

R&S®RTP-K21 USB 2.0 compliance test

The option is used in combination with the free-of-charge R&S®ScopeSuite PC software, which can be downloaded from the Rohde & Schwarz website. R&S®RTP-K21 performs USB 2.0 compliance test measurements with R&S®ScopeSuite, including tests for USB 2.0 (high speed), USB 1.1 (full speed) and USB 1.0 (low speed) with the R&S®RTP. R&S®ScopeSuite supports the R&S®RT-ZF1 USB 2.0 compliance test fixture set and the Allion USB test fixture solutions and the USB-IF signal quality board device/host.

Supported USB 2.0 compliance tests		
USB device test	high speed	signal quality (EL_2, 4, 5, 6, 7); packet parameters (EL_21, 22, 25); chirp timing (EL_28, 29, 31); suspend/resume/reset timing (EL_27, 28, 38, 39, 40); test J/K, SE0_NAK (EL_8, 9); receiver sensitivity (EL_16, 17, 18)
	full speed and low speed	full speed signal quality; back voltage; inrush current
USB host test	high speed	signal quality (EL_2, 3, 6, 7); packet parameters (EL_21, 22, 23, 25, 55); chirp timing (EL_33, 34, 35); suspend/resume/reset timing (EL_39, 41); test J/K, SE0_NAK (EL_8, 9)
	full speed and low speed	low speed signal quality downstream; full speed signal quality downstream; drop; droop
USB hub test	high speed	signal quality upstream (EL_2, 4, 6, 7); signal quality downstream (EL_2, 3, 6, 7); jitter downstream (EL_47); packet parameters upstream (EL_21, 22, 25); hub receiver sensitivity upstream (EL_16, 17, 18); repeater downstream (EL_42, 43, 44, 45, 48); repeater upstream (EL_42, 43, 44, 45); chirp timing upstream (EL_28, 29, 31); suspend/resume/reset timing upstream (EL_27, 28, 38, 39, 40); test J/K, SE0_NAK upstream (EL_8, 9); test J/K, SE0_NAK downstream (EL_8, 9)
	full speed and low speed	low speed signal quality downstream; full speed signal quality upstream; full speed signal quality downstream; inrush current upstream; drop downstream; droop downstream; back voltage

R&S®RTP-K22 Ethernet compliance test (10/100/1000BASE-T/EEE)

The option is used in combination with the free-of-charge R&S®ScopeSuite PC software, which can be downloaded from the Rohde & Schwarz website. R&S®RTP-K22 performs Ethernet compliance test measurements with R&S®ScopeSuite, including tests for 10BASE-T, 100BASE-TX,1000BASE-T and energy efficient Ethernet (EEE) with the R&S®RTP. R&S®ScopeSuite supports the R&S®RT-ZF2 Ethernet compliance test fixture set as well as the R&S®RT-ZF4 and R&S®RT-ZF5 for EEE.

Supported Ethernet compliance tests		
Standard reference		IEEE 802.3-2012
1000BASE-T	with/without disturber	with/without TX_CLK transmitter distortion (40.6.1.2.4)
		peak differential output voltage (40.6.1.2.1)
		maximum output droop (40.6.1.2.2)
		differential output templates (40.6.1.2.3)
	with TX_CLK	jitter master mode (40.6.1.2.5), jitter slave mode (40.6.1.2.5)
	without TX_CLK	jitter master mode (40.6.1.2.5)
	common	MDI return loss (40.8.3.1), common mode output voltage (40.8.3.3)
100BASE-TX		amplitude domain tests (9.1.2.2, 9.1.3 and 9.1.4)
		rise and fall times (9.1.6)
		peak to peak duty cycle distortion (9.1.8)
		peak to peak transmitter jitter (9.1.9)
		active output interface template (annex J)
		transmitter return loss (9.1.5)
		receiver return loss (9.2.2)
10BASE-T	no TPM	link test pulse template (14.3.1.2.1)
		TP_IDL template (14.3.1.2.1)
		peak differential voltage (14.3.1.2.1)
		harmonic content (14.3.1.2.1)
		output timing jitter (14.3.1.2.3)
	with TPM	link test pulse template (14.3.1.2.1)
		TP_IDL template (14.3.1.2.1)
		MAU template (14.3.1.2.1)
		output timing jitter (14.3.1.2.3)
	common	transmitter return loss (14.3.1.2.2), receiver return loss (14.3.1.3.4)
		common mode output voltage (14.3.1.2.5)

Supported EEE compliance tests		
Standard reference		IEEE 802.3-2012
1000BASE-T EEE (requires R&S®RT-ZF5)		quiet time (78.2)
		refresh time (master) (78.2)
		refresh time (slave) (78.2)
		wake state levels (40.6.1.2.7)
		transmitter timing jitter with TX_TCLK (master) (40.6.1.2.5)
		transmitter timing jitter with TX_TCLK (slave) (40.6.1.2.5)
		transmitter timing jitter without TX_TCLK (master) (40.6.1.2.5)
		transmitter timing jitter without TX_TCLK (master) (40.6.1.2.5)
100BASE-TX EEE (requires R&S®RT-ZF5)		sleep time (24.2.3.4 and 78.2)
		LPI quiet time (24.2.3.4 and 78.2)
		LPI refresh time (24.2.3.4 and 78.2)
		LPI transmitter timing jitter (24.2.3.4 and 78.2)
		transmit wake time (24.2.3.4 and 78.2)

10BASE-Te (requires R&S®RT-ZF4)	no TPM	link test pulse template (14.3.1.2.1)
		TP_IDL template (14.3.1.2.1)
		peak differential voltage (14.3.1.2.1)
		harmonic content (14.3.1.2.1)
		output timing jitter (14.3.1.2.3)
	with TPM	link test pulse template (14.3.1.2.1)
		TP_IDL template (14.3.1.2.1)
		MAU template (14.3.1.2.1)
		output timing jitter (14.3.1.2.3)
	common	transmitter return loss (14.3.1.2.2), receiver return loss (14.3.1.3.4)
		common mode output voltage (14.3.1.2.5)

R&S®RTP-K23 Ethernet compliance test (2.5/5/10GBASE-T)

The option is used in combination with the free-of-charge R&S®ScopeSuite PC software, which can be downloaded from the Rohde & Schwarz website. R&S®RTP-K23 performs Ethernet compliance test measurements with the R&S®ScopeSuite, including tests for 2.5GBASE-T, 5GBASE-T and 10GBASE-T with the R&S®RTP. R&S®ScopeSuite supports the R&S®RT-ZF2 Ethernet compliance test fixture set.

Supported Ethernet compliance tests		
Standard reference		IEEE 802.3-2012 and IEEE P802.3bz
2.5/5GBASE-T		maximum output droop (126.5.3.1)
		transmitter nonlinear distortion (126.5.3.2)
		transmitter timing jitter master mode and clock frequency (126.5.3.3 and 126.5.3.5)
		transmitter timing jitter slave mode (126.5.3.3)
		transmitter power spectral density and power level (126.5.3.4)
		MDI return loss (126.6.2.1)
10GBASE-T		maximum output droop (55.5.3.1)
		transmitter linearity (55.5.3.2)
		transmitter timing jitter master mode (55.5.3.3)
		transmitter timing jitter slave mode (55.5.3.3)
		transmitter power spectral density (55.5.3.4)
		transmitter power level (55.5.3.4)
		transmitter clock frequency (55.5.3.5)
		MDI return loss (55.8.2.1)

R&S®RTP-K24 Ethernet compliance test (100BASE-T1)

The option is used in combination with the free-of-charge R&S®ScopeSuite PC software, which can be downloaded from the Rohde & Schwarz website. R&S®RTP-K24 performs 100BASE-T1 compliance test measurements with R&S®ScopeSuite. R&S®ScopeSuite supports the R&S®RT-ZF2, R&S®RT-ZF7A and R&S®RT-ZF8 Ethernet compliance test fixtures. The chapters after the test cases refer to IEEE 802.3-2018 and OPEN Alliance ECU specification version 2.0.

Supported Ethernet compliance tests		
100BASE-T1		transmitter output droop (96.5.4.1)
		transmitter distortion with and without disturber (96.5.4.2)
		transmitter timing jitter master mode (96.5.4.3)
		transmitter timing jitter slave mode (96.5.4.3)
		transmitter power spectral density (96.5.4.4)
		transmitter clock frequency (96.5.4.5)
		transmitter peak differential output (96.5.6)
		MDI return loss (96.7.1.3)
		MDI mode conversion loss (96.8.2.2)
		MDI mode conversion loss adapter verification (OABR_PMA_TX_06)
		MDI common mode emission (OABR_PMA_TX_07)

R&S®RTP-K26 MIPI D-PHY compliance test

The option is used in combination with the free-of-charge R&S®ScopeSuite PC software, which can be downloaded from the Rohde & Schwarz website. R&S®RTP-K26 performs D-PHY compliance test measurements with R&S®ScopeSuite. The numbers behind the test refer to the MIPI CTS for D-PHY V1.1 and V1.2.

Supported D-PHY compliance tests		
D-PHY	group 1 (7 tests): data lane LP-TX signaling requirements	data lane LP-TX Thevenin output high level voltage (V_{OH}) – 1.1.1
		data lane LP-TX Thevenin output low level voltage (V_{OL}) – 1.1.2
		data lane LP-TX from 15 % to 85 % rise time (T_{RLP}) – 1.1.3
		data lane LP-TX from 85 % to 15 % fall time (T_{FLP}) – 1.1.4
		data lane LP-TX slew rate versus C_{LOAD} ($\delta V/\delta t_{SR}$) – 1.1.5
		data lane LP-TX pulse width of exclusive-OR clock ($T_{LP\text{-}PULSE\text{-}TX}$) – 1.1.6
		data lane LP-TX period of exclusive-OR clock ($T_{LP\text{-}PER\text{-}TX}$) – 1.1.7
	group 2 (5 tests): clock lane LP-TX signaling requirements	clock lane LP-TX Thevenin output high level voltage (V_{OH}) – 1.2.1
		clock lane LP-TX Thevenin output low level voltage (V_{OL}) – 1.2.2
		clock lane LP-TX from 15 % to 85 % rise time (T_{RLP}) – 1.2.3
		clock lane LP-TX from 85 % to 15 % fall time (T_{FLP}) – 1.2.4
		clock lane LP-TX slew rate versus C_{LOAD} ($\delta V/\delta t_{SR}$) – 1.2.5
	group 3 (16 tests): data lane HS-TX signaling requirements	data lane HS entry: data lane T_{LPX} value – 1.3.1
		data lane HS entry: data lane $T_{HS\text{-}PREPARE}$ value – 1.3.2
		data lane HS entry: data lane $T_{HS\text{-}PREPARE} + T_{HS\text{-}ZERO}$ value – 1.3.3
		data lane HS-TX differential voltages $V_{OD(0)}$ and $V_{OD(1)}$ – 1.3.4
		data lane HS-TX differential voltage mismatch ΔV_{OD} – 1.3.5
		data lane HS-TX single-ended output voltages $V_{OHHS(DP)}$ and $V_{OHHS(DN)}$ – 1.3.6
		data lane HS-TX static common mode voltages $V_{CMTX(1)}$ and $V_{CMTX(0)}$ – 1.3.7
		data lane HS-TX static common mode voltage mismatch $\Delta V_{CMTX(1.0)}$ – 1.3.8
		data lane HS-TX dynamic common-level variations from 50 MHz to 450 MHz $\Delta V_{CMTX(LF)}$ – 1.3.9
		data lane HS-TX dynamic common-level variations above 450 MHz $\Delta V_{CMTX(HF)}$ – 1.3.10
		data lane HS-TX from 20 % to 80 % rise time t_R – 1.3.11
		data lane HS-TX from 80 % to 20 % fall time t_F – 1.3.12
		data lane HS exit: $T_{HS\text{-}TRAIL}$ value – 1.3.13
		data lane HS exit: from 30 % to 85 % post-EoT rise time T_{REOT} – 1.3.14
		data lane HS exit: T_{EOT} value – 1.3.15
		data lane HS exit: $T_{HS\text{-}EXIT}$ value – 1.3.16

D-PHY	group 4 (18 tests): clock lane HS-TX signaling requirements	clock lane HS entry: T_{LPX} value – 1.4.1
		clock lane HS entry: $T_{CLK-PREPARE}$ value – 1.4.2
		clock lane HS entry: $T_{CLK-PREPARE}$ + $T_{CLK-ZERO}$ value – 1.4.3
		clock lane HS-TX differential voltages $V_{OD(0)}$ and $V_{OD(1)}$ – 1.4.4
		clock lane HS-TX differential voltage mismatch ΔV_{OD} – 1.4.5
		clock lane HS-TX single-ended output voltages $V_{OHHS(DP)}$ and $V_{OHHS(DN)}$ – 1.4.6
		clock lane HS-TX static common mode voltages $V_{CMTX(1)}$ and $V_{CMTX(0)}$ – 1.4.7
		clock lane HS-TX static common mode voltage mismatch $\Delta V_{CMTX(1, 0)}$ – 1.4.8
		clock lane HS-TX dynamic common-level variations from 50 MHz to 450 MHz $\Delta V_{CMTX(LF)}$ – 1.4.9
		clock lane HS-TX dynamic common-level variations above 450 MHz $\Delta V_{CMTX(HF)}$ – 1.4.10
		clock lane HS-TX from 20 % to 80 % rise time t_R – 1.4.11
		clock lane HS-TX from 80 % to 20 % fall time t_F – 1.4.12
		clock lane HS exit: $T_{CLK-TRAIL}$ value – 1.4.13
		clock lane HS exit: from 30 % to 85 % post-EoT rise time T_{REOT} – 1.4.14
		clock lane HS exit: T_{EOT} value – 1.4.15
		clock lane HS exit: $T_{HS-EXIT}$ value – 1.4.16
		clock lane HS clock instantaneous: UI_{INST} value – 1.4.17
		clock lane HS clock delta UI: (ΔUI) value – 1.4.18
	group 5 (6 tests): HS-TX clock-to-data lane timing requirements	HS entry: $T_{CLK-PRE}$ value – 1.5.1
		HS exit: $T_{CLK-POST}$ value – 1.5.2
		HS clock rising edge alignment to first payload bit – 1.5.3
		data-to-clock skew ($T_{SKEW[TX]}$) – 1.5.4
		initial HS skew calibration burst $T_{SKEWCAL-SYNC}$ $T_{SKEWCAL}$– 1.5.5
		periodic HS skew calibration burst $T_{SKEWCAL-SYNC}$ $T_{SKEWCAL}$– 1.5.6

R&S®RTP-K27 MIPI D-PHY 2.5 compliance test

The option is used in combination with the free-of-charge R&S®ScopeSuite PC software, which can be downloaded from the Rohde & Schwarz website. R&S®RTP-K27 performs D-PHY2 compliance test measurements with R&S®ScopeSuite. The numbers behind the test refer to the MIPI CTS for D-PHY V2.0, V2.1 and V2.5.

Supported D-PHY compliance tests		
D-PHY	group 1 (7 tests): data lane LP-TX signaling requirements	data lane LP-TX Thevenin output high level voltage (V_{OH}) – 1.1.1
		data lane LP-TX Thevenin output low level voltage (V_{OL}) – 1.1.2
		data lane LP-TX from 15 % to 85 % rise time (T_{RLP}) – 1.1.3
		data lane LP-TX from 85 % to 15 % fall time (T_{FLP}) – 1.1.4
		data lane LP-TX slew rate versus C_{LOAD} ($\delta V/\delta t_{SR}$) – 1.1.5
		data lane LP-TX pulse width of exclusive-OR clock ($T_{LP\text{-}PULSE\text{-}TX}$) – 1.1.6
		data lane LP-TX period of exclusive-OR clock ($T_{LP\text{-}PER\text{-}TX}$) – 1.1.7
	group 2 (5 tests): clock lane LP-TX signaling requirements	clock lane LP-TX Thevenin output high level voltage (V_{OH}) – 1.2.1
		clock lane LP-TX Thevenin output low level voltage (V_{OL}) – 1.2.2
		clock lane LP-TX from 15 % to 85 % rise time (T_{RLP}) – 1.2.3
		clock lane LP-TX from 85 % to 15 % fall time (T_{FLP}) – 1.2.4
		clock lane LP-TX slew rate versus C_{LOAD} ($\delta V/\delta t_{SR}$) – 1.2.5
	group 3 (16 tests): data lane HS-TX signaling requirements	data lane HS entry: data lane T_{LPX} value – 1.3.1
		data lane HS entry: data lane $T_{HS\text{-}PREPARE}$ value – 1.3.2
		data lane HS entry: data lane $T_{HS\text{-}PREPARE}$ + $T_{HS\text{-}ZERO}$ value – 1.3.3
		data lane HS-TX differential voltages $V_{OD(0)}$ and $V_{OD(1)}$ – 1.3.4
		data lane HS-TX differential voltage mismatch ΔV_{OD} – 1.3.5
		data lane HS-TX single-ended output voltages $V_{OHHS(DP)}$ and $V_{OHHS(DN)}$ – 1.3.6
		data lane HS-TX static common mode voltages $V_{CMTX(1)}$ and $V_{CMTX(0)}$ – 1.3.7
		data lane HS-TX static common mode voltage mismatch $\Delta V_{CMTX(1.0)}$ – 1.3.8
		data lane HS-TX dynamic common-level variations from 50 MHz to 450 MHz $\Delta V_{CMTX(LF)}$ – 1.3.9
		data lane HS-TX dynamic common-level variations above 450 MHz $\Delta V_{CMTX(HF)}$ – 1.3.10
		data lane HS-TX from 20 % to 80 % rise time t_R – 1.3.11
		data lane HS-TX from 80 % to 20 % fall time t_F – 1.3.12
		data lane HS exit: $T_{HS\text{-}TRAIL}$ value – 1.3.13
		data lane HS exit: from 30 % to 85 % post-EoT rise time T_{REOT} – 1.3.14
		data lane HS exit: T_{EOT} value – 1.3.15
		data lane HS exit: $T_{HS\text{-}EXIT}$ value – 1.3.16

D-PHY	group 4 (19 tests): clock lane HS-TX signaling requirements	clock lane HS entry: T_{LPX} value – 1.4.1
		clock lane HS entry: $T_{CLK-PREPARE}$ value – 1.4.2
		clock lane HS entry: $T_{CLK-PREPARE}$ + $T_{CLK-ZERO}$ value – 1.4.3
		clock lane HS-TX differential voltages $V_{OD(0)}$ and $V_{OD(1)}$ – 1.4.4
		clock lane HS-TX differential voltage mismatch ΔV_{OD} – 1.4.5
		clock lane HS-TX single-ended output voltages $V_{OHHS(DP)}$ and $V_{OHHS(DN)}$ – 1.4.6
		clock lane HS-TX static common mode voltages $V_{CMTX(1)}$ and $V_{CMTX(0)}$ – 1.4.7
		clock lane HS-TX static common mode voltage mismatch $\Delta V_{CMTX(1, 0)}$ – 1.4.8
		clock lane HS-TX dynamic common-level variations from 50 MHz to 450 MHz $\Delta V_{CMTX(LF)}$ – 1.4.9
		clock lane HS-TX dynamic common-level variations above 450 MHz $\Delta V_{CMTX(HF)}$ – 1.4.10
		clock lane HS-TX from 20 % to 80 % rise time t_R – 1.4.11
		clock lane HS-TX from 80 % to 20 % fall time t_F – 1.4.12
		clock lane HS exit: $T_{CLK-TRAIL}$ value – 1.4.13
		clock lane HS exit: from 30 % to 85 % post-EoT rise time T_{REOT} – 1.4.14
		clock lane HS exit: T_{EOT} value – 1.4.15
		clock lane HS exit: $T_{HS-EXIT}$ value – 1.4.16
		clock lane HS clock instantaneous: UI_{INST} value – 1.4.17
		clock lane HS clock delta UI: (ΔUI) value – 1.4.18
		TX spread spectrum clocking (SSC) requirements (1.4.19)
	group 5 (9 tests): HS-TX clock-to-data lane timing requirements	HS entry: $T_{CLK-PRE}$ value – 1.5.1
		HS exit: $T_{CLK-POST}$ value – 1.5.2
		HS clock rising edge alignment to first payload bit – 1.5.3
		data-to-clock skew ($T_{SKEW[TX]}$) – 1.5.4
		initial HS skew calibration burst $T_{SKEWCAL-SYNC}$ $T_{SKEWCAL}$– 1.5.5
		periodic HS skew calibration burst $T_{SKEWCAL-SYNC}$ $T_{SKEWCAL}$– 1.5.6
		alternate calibration sequence $T_{ALTCAL-SYNC}$ and T_{ALTCAL} – 1.5.8
		preamble sequence $T_{PREAMBLE}$ and $T_{EXTSYNC}$ – 1.5.9
		clock and data lane TX HS-Idle $T_{HS-IDLE-POST}$, $T_{HS-IDLE-CLKHS0}$, $T_{HS-IDLE-PRE}$ – 1.5.10
	eye test (3 tests)	clock lane HS clock delta UI (ΔUI) –1.4.18
		clock lane HS clock period jitter –1.4.20
		HS-TX data and clock eye diagram –1.5.7
Requirements		
Options	R&S®RTP-K136 (max. 8 Gbps) or R&S®RTP-K137 (max. 16 Gbps)	advanced eye analysis

R&S®RTP-K28 MIPI C-PHY compliance test

The option is used in combination with the free-of-charge R&S®ScopeSuite PC software, which can be downloaded from the Rohde & Schwarz website. R&S®RTP-K28 performs C-PHY compliance test measurements with R&S®ScopeSuite. The numbers behind the test refer to the MIPI CTS for C-PHY V1.2 and V2.1.

Supported C-PHY compliance tests		
C-PHY	group 1 (8 tests): data lane LP-TX signaling requirements	data lane LP-TX Thevenin output high level voltage (V_{OH}) – 1.1.1
		data lane LP-TX Thevenin output low level voltage (V_{OL}) – 1.1.2
		data lane LP-TX from 15 % to 85 % rise time (T_{RLP}) – 1.1.3
		data lane LP-TX from 85 % to 15 % fall time (T_{FLP}) – 1.1.4
		data lane LP-TX slew rate versus C_{LOAD} ($\delta V/\delta t_{SR}$) – 1.1.5
		data lane LP-TX pulse width of exclusive-OR clock ($T_{LP\text{-}PULSE\text{-}TX}$) – 1.1.6
		data lane LP-TX period of exclusive-OR clock ($T_{LP\text{-}PER\text{-}TX}$) – 1.1.7
		data lane $T_{LP\text{-}EXIT}$ – 1.1.8
	group 2 (17 tests): data lane HS-TX signaling requirements	data lane HS entry: data lane T_{LPX} value – 1.2.1
		data lane HS entry: data lane $T_{3\text{-}PREPARE}$ value – 1.2.2
		data lane HS entry: data lane $T_{3\text{-}PREBEGIN}$ value – 1.2.3
		data lane HS entry: data lane $T_{3\text{-}PROGSEQ}$ value – 1.2.4
		data lane HS entry: data lane $T_{3\text{-}PREEND}$ value – 1.2.5
		data lane HS entry: data lane $T_{3\text{-}SYNC}$ value – 1.2.6
		data lane HS-TX static common mode voltages V_{CPTX} – 1.2.10
		data lane HS-TX static common mode voltage mismatch $\Delta V_{CPTX(HS)}$ – 1.2.11
		data lane HS-TX dynamic common-level variations from 50 MHz to 450 MHz $\Delta V_{CPTX(LF)}$ – 1.2.12
		data lane HS-TX dynamic common-level variations above 450 MHz $\Delta V_{CPTX(HF)}$ – 1.2.13
		data lane HS-TX rise time t_R – 1.2.14
		data lane HS-TX fall time t_F – 1.2.15
		data lane $T_{3\text{-}POST}$ duration – 1.2.16
		data lane HS exit: from 30 % to 85 % post-EoT rise time T_{REOT} – 1.2.17
		data lane HS exit: $T_{HS\text{-}EXIT}$ value – 1.2.18
		data lane HS clock instantaneous UI UI_{inst} value – 1.2.19
		data lane HS clock delta UI ΔUI value – 1.2.20
	group 2 (5 tests): data lane HS-TX signaling requirements eye test	data lane HS-TX differential voltages V_{OD_AB}, V_{OD_BC} and V_{CA} – 1.2.7
		data lane HS-TX differential voltage mismatch ΔV_{OD} – 1.2.8
		data lane HS-TX single-ended output voltages $V_{OHHS(AB)}$, $V_{OHHS(BC)}$ and $V_{OHHS(CA)}$ – 1.2.9
		data lane TX eye diagram test – 1.2.21
		data lane HS-TX UI jitter $UI\_Jitter_{peak+tx}$ value – 1.2.22
Requirements		
Options	R&S®RTP-K136 (max. 8 Gbps) or R&S®RTP-K137 (max. 16 Gbps)	advanced eye analysis

R&S®RTP-K35 bus analysis

General description	The R&S®RTP-K35 bus analysis option adds bus measurements and analysis functions for dedicated protocols.	
	supported protocol options	R&S®RTP-K1 (I^2C, SPI), R&S®RTP-K2 (UART), R&S®RTP-K3 (CAN, LIN), R&S®RTP-K8 (Ethernet), R&S®RTP-K9 (CAN-FD), R&S®RTP-K40 (RFFE), R&S®RTP-K57 (100BASE-T1)
Measurements	field value	allows the selection of frame types and displays the value of a specified field; the value can be displayed as track and histogram
	frame to frame	measures the distance between the starts of two selectable frame types in seconds
	trigger to frame	measures the distance between the trigger event and the start of a selectable frame type in seconds; alternatively, measures the distance between the start of a selectable frame type and the trigger event
	frame count	counts the total number of frames in each acquisition
	gap time	measures the distance between the end of a selectable frame type to the start of another selectable frame type in seconds
	bus idle ratio	measures the percentage of idle time on a bus; idle time is defined as the time where the bus is not occupied by frames
	main bit rate	measures the main bit rate of a protocol based on the relevant bits in a frame; if a protocol provides multiple bit rates, the most relevant bit rate is being measured
	secondary bit rate	for protocols with multiple bit rates, the secondary bit rate is available
	frame error count	counts the total number of erroneous frames in each acquisition
	frame error rate	measures the percentage of erroneous frames in relation to the total frames
	consecutive frame error rate	measures the percentage of follow up (consecutive) frame errors, ignoring all single frame errors

R&S®RTP-K37 spectrogram

General description	The R&S®RTP-K37 spectrogram option allows advanced signal analysis in the frequency domain by visualization of the frequency spectrum versus time.	
Spectrogram	display characteristics	spectrogram display; a separate spectrogram can be created for each FFT display; each FFT segment of a captured acquisition is displayed in a separate spectrogram line
		support of logarithmic frequency x-axis
	number of spectrograms	up to 4
	signal colors	predefined or user-defined color tables for persistence display with the spectrogram
	timelines	in stop mode two separate timelines can be used to navigate through a spectrogram in time; for each timeline the relevant FFT segment is displayed in a diagram; the difference in acquisition time between the timelines is displayed
	measurements	THD_a, THD_u, THD_r

R&S®RTP-K39 user-defined math

General description	The R&S®RTP-K39 user-defined math option provides a Python interface to apply user functions defined by Python scripts to the waveform processing. The output can be visualized as a waveform math signal.

R&S®RTP-K40 MIPI RFFE serial triggering and decoding

Protocol configuration	signal type	two channel, single-ended
	bit rate	auto-detected
	auto threshold setup	assisted threshold configuration
	full autoset	full autoset of horizontal and vertical settings and auto threshold setup
	source (SCLK, SDATA)	any two input channels, math waveforms, reference waveforms or logical channels
	supported version	1.X, 2.0, 2.1 and 3.0
	read mode	standard or sRead mode
	glitch filter	configurable glitch filter
	gap detection	detect gaps between sequences
Trigger	trigger event setup	sequence start, sequence stop, register 0 write, register write, register read, extended register write, extended register read, extended register write long, extended register read long, error condition types
	sequence start setup	4 bit slave address; conditions =, ≠, <, ≤, >, ≥, in range, out of range
	sequence stop setup	4 bit slave address; conditions =, ≠, <, ≤, >, ≥, in range, out of range
	register 0 write setup	4 bit slave address, 7 bit data word; conditions =, ≠, <, ≤, >, ≥, in range, out of range for each of these options
	register write/read	4 bit slave address, 5 bit register address, 8 bit data word; conditions =, ≠, <, ≤, >, ≥, in range, out of range for each of these options
	extended register write/read	4 bit slave address; 8 bit address, byte count: 0 to 15 (inclusive), data pattern: 1 byte to 16 byte (hex or binary); conditions =, ≠, <, ≤, >, ≥, in range, out of range for each of these options; index: 1 to 16 selects the specific data frame byte; conditions =, ≠, <, ≤, >, ≥, in range
	extended register write long/read long	4 bit slave address, 8 bit address, byte count: 0 to 7 (inclusive), data pattern: 0 to 8 byte (hex or binary); conditions =, ≠, <, ≤, >, ≥, in range, out of range for each of these options; index: 1 to 8 selects the specific data frame byte; conditions =, ≠, <, ≤, >, ≥, in range
	interrupt summary and notification	4 bit slave address, bit count 0 to 32, notification and interrupt bits
	masked write	4 bit slave address; 8 bit address, 8 bit mask, 8 bit data pattern; conditions =, ≠, <, ≤, >, ≥, in range, out of range for each of these options; frame byte; conditions =, ≠, <, ≤, >, ≥, in range
	master ownership handover	2 bit MID; conditions =, ≠, <, ≤, >, ≥, in range, out of range for each of these options; frame byte; conditions =, ≠, <, ≤, >, ≥, in range

	master write/read	2 bit MID, 8 bit address, 16 bit data pattern; conditions =, ≠, <, ≤, >, ≥, in range, out of range for each of these options; frame byte; conditions =, ≠, <, ≤, >, ≥, in range
	master context transfer write/read	2 bit MID, 8 bit byte count, 8 bit address, data pattern: 1 byte to 8 byte (hex or binary); conditions =, ≠, <, ≤, >, ≥, in range, out of range for each of these options; index: 1 to 256 selects the specific data frame byte; conditions =, ≠, <, ≤, >, ≥, in range
	error condition	SSC error; length error, bus park error, parity error, no response, unknown sequence, version error, min. gap between frames: 1 ns to 10 us
Decode	display type	decoded bus, logical signal, bus + logical signal, tabulated list, decode layers
	color coding	sequence, frame, error
	data format	hex, octal, binary, signed, unsigned
	decode layer	off, edges, bit
	result export	export of all result data into CSV, XML, HTML and PY file formats
Search	search event setup	sequence start, sequence stop, register 0 write, register write, register read, extended register write, extended register read, extended register write long, extended register read long, master read, master write, master ownership handover, interrupt summary and notification, error condition types
	event settings	same as trigger event settings

R&S®RTP-K42 MIPI D-PHY serial triggering and decoding

Protocol configuration	signal type	clock, data (differential or single-ended)
	bit rate	selectable without clock lane (1 Mbps to 2.5 Gbps), auto detect with clock lane
	source	any input channels, math waveforms, reference waveforms
	variants	D-PHY v. 1.2, CSI-2 v.1.2, DSI v. 1.3
Trigger	trigger event setup	HS start of packet
		HS end of packet
		HS packet header
		HS data
		LP escape mode
		LP lane turnaround
		LP HS request
	HS packet header setup	virtual channel, data type, word count; conditions =, ≠, <, ≤, >, ≥, in range, out of range for data and word count
	HS data	virtual channel, data type, word count, data value, data index; conditions =, ≠, <, ≤, >, ≥, in range, out of range for data count, word count, data value
	LP escape mode	escape mode, data value, data index; conditions =, ≠, <, ≤, >, ≥, in range, out of range for escape mode and data value

Decode	display type	decoded bus, tabulated list, details, decode layers
	color coding	high speed: frames according to trace, cells; low power: escape word, data word
	data format	hex, octal, binary, signed, unsigned
	decode layer	off, HS edges, HS binary, HS burst bit, HS burst byte, HS merged byte, HS merged words, LP edges, LP states, LP active states, LP binary
	result export	export of all result data into CSV, XML, HTML and PY file formats
Search	search event setup	HS start of packet
		HS end of packet
		HS packet header
		HS data
		LP escape mode
		LP lane turnaround
		LP HS request
	event settings	same as trigger event setup

R&S®RTP-K44 MIPI M-PHY serial triggering and decoding

Protocol configuration	signal type	up to 4 channels, differential
	bit rate	clock recovery
	source (SDATA)	analog and math channels, reference waveforms
	variants	UniPro 1.6 and M-PHY 4.0
Trigger	trigger event setup	M-PHY burst
		M-PHY adapt
		M-PHY LCC
		UniPro DL_PDU frames
		UniPro PACP frames
		UniPro trigger upper frames
		M-PHY/UniPro errors
Decode	display type	decoded bus, logical signal, bus + logical signal, tabulated list, details, decode layers
	color coding	for different cells/frame types
	data format	K/D symbols; with UniPro additionally: hex, octal, binary, signed, unsigned
	decode layer	off, edges, bit, 8b10b synbols, LCC bit; with UniPro additionally: filter/descrambler, lane merge, byte
Search	search event setup	M-PHY burst
		M-PHY adapt
		M-PHY LCC
		UniPro DL_PDU frames
		UniPro PACP frames
		UniPro trigger upper frames
		M-PHY/UniPro errors

R&S®RTP-K50 Manchester and NRZ serial triggering and decoding

Protocol configuration	signal type	selectable, one channel, differential or single-ended, two channel, differential or single-ended
	bit rate	auto detected, adjustable
	auto threshold setup	assisted threshold configuration
	source	analog, math. channels, logical (only NRZ)
	bit encoding variants	Manchester, Manchester II, NRZ clocked, NRZ unclocked
	properties	active state (high/low), idle state (high/low), clock edge (first/second)
	frame separation	gap, enable signal (only NRZ)
Frame format	frame	multiple frame management, frame identification and sync, variable length frames, variable number of cells
	cells	name, size (bit), numeric format, bit order, color
	file storage of frame format	save/load as xml files
Trigger	variants	all supported bit encodings
	trigger event setup	frame start
		pattern
		advanced trigger
	frame start	gap, start bit
	pattern	up to 256 bit pattern within 65 535 bit frame
	advanced trigger	frame type (with OR combinations), frame fields (with AND combinations), frame field data; conditions =, ≠, <, ≤, >, ≥, in range, out of range for data count, word count, data value; error types
Decode	display type	decoded bus, logical signal, bus signal, tabulated list, result details, decode layers
	color coding	according to cell configuration table
	data format	according to cell configuration table
	decode layer	edges, binary
Search	event settings	same as advanced trigger settings
Filter	The filter function selects those decode events that shall be shown in the result table. Events that do not match the criteria set will not be displayed in the table when the filter is turned on.	
	settings	same as advanced trigger settings

R&S®RTP-K52 8b10b serial triggering and decoding

Protocol configuration	signal type	one/two channel, differential, single-ended
	bit rate	selectable/adjustable auto configuration
	auto threshold setup	assisted threshold configuration
	one click setup	convenient way for perfect decode results; auto scaling of waveforms, auto threshold and bitrate estimation on one click
	source (differential, single-ended D+/D–)	full combination of either analog, math, reference channels
	variants	all layer 1 (physical layer) encoded 8b10b protocols, recommended for Ethernet, FibreChannel 1G, 2G, PCI Express, Serial ATA, Serial Rapid IO (SRIO), XAUI
Trigger	trigger event setup	symbols, errors
	symbols	K/D symbol (8 bit/10 bit), complex expression (combination of K/D symbols, wildcards, disparity)
	errors	disparity, glitching and unknown symbol

Decode	display type	decoded bus, bus signal, tabulated list, details, decode layers
	color coding	sync symbol, K symbols, data (Dx.y) coding and error coding
	data format	hex, 10 bit and K/D representation
	decode layer	edges, bit
Search	search event setup	symbols, errors
	event settings	same as trigger event settings

R&S®RTP-K55 MDIO serial triggering and decoding

Protocol configuration	bit rate	up to 5 Mbps (auto-detected)
	auto threshold setup	assisted threshold configuration for MDIO triggering and decoding
	device list	associate frame address with symbolic ID
Trigger	source (clock and data)	any input channel or logical channel
	trigger event setup	start, stop, ST, OP, PHY address, register address, data
	ST setup	01 (clause 22), 00 clause 45, any
	OP setup	address, write, post read, read, any
	PHY address setup	5 bit address (hex, decimal, octal or binary); equal
	PHY register (clause 22)/device type (clause 45) setup	5 bit value (hex, decimal, octal or binary); equal
	data (clause 22)/data/address (clause 45)	16 bit value (hex, decimal, octal or binary); equal
Decode	source (clock and data)	any input channel, math waveform, reference waveform, logical channel
	display type	decoded bus, logical signal, bus + logical signal, tabulated list, decode layers
	color coding	frame, PHY address, PHY register, address, data, turnaround
	PHYAD/PRTAD	symbolic names for user-defined addresses
	address/data field format	hex, decimal, octal, binary, ASCII, signed, unsigned
	decode layer	final, edges, binary
Search	source (clock and data)	any input channel, math waveform, reference waveform, logical channel
	search event setup	start, stop, ST, OP, PHY address, register address, data
	event settings	same as trigger event settings

R&S®RTP-K57 Ethernet (100BASE-T1) serial triggering and decoding

Protocol configuration	signal type	one channel differential, two channels single-ended, optional additional use of reverse channels for signal improvement: one channel differential, two channels single-ended
	symbol rate	66.667 Msymbol/s, adjustable for testing
	thresholds	upper/lower, assisted threshold configuration
	source	any analog input channels, math waveforms, reference waveforms
	polarity	normal, inverted
	mode	slave, master
Trigger	trigger event setup	frame start
		MAC frame
		idle frame
		error conditions
	MAC frame setup	destination address (condition =, ≠, <, >, ≥, ≤, in range, out of range), source address (condition =, ≠, <, >, ≥, ≤, in range, out of range), length/type (condition =, ≠, <, >, ≥, ≤, in range, out of range), frame check (condition =, ≠, <, >, ≥, ≤, in range, out of range), data (condition =, ≠, <, >, ≥, ≤, in range, out of range), data index (condition =, <, >, ≥, ≤, range)
	error condition setup	preamble error, CRC error, SFD error
Decode	display type	decoded bus, tabulated list, details, decode layers
	color coding	for different cell types
	data format	hex, octal, binary, signed, unsigned
	decode layer	reversed bit, descrambled bit, scrambled bit, ternary symbols
	result export	export of all result data into CSV, XML, HTML and PY file formats
Search	search event setup	frame start
		MAC frame
		idle frame
		error conditions
	event settings	same as trigger event settings

R&S®RTP-K58 Ethernet (1000BASE-T1) serial triggering and decoding

Protocol configuration	signal type	one channel differential, two channels single-ended, optional additional use of reverse channels for signal improvement: one channel differential, two channels single-ended
	symbol rate	750 Msymbol/s, adjustable for testing
	thresholds	automatically adjusted during decoding
	source	any analog input channels, math waveforms, reference waveforms
	polarity	normal, inverted
	mode	slave, master
Trigger	trigger event setup	frame start
		MAC frame
		idle frame
		error conditions
	MAC frame setup	destination address (condition =, ≠, <, >, ≥, ≤, in range, out of range), source address (condition =, ≠, <, >, ≥, ≤, in range, out of range), length/type (condition =, ≠, <, >, ≥, ≤, in range, out of range), frame check (condition =, ≠, <, >, ≥, ≤, in range, out of range), data (condition =, ≠, <, >, ≥, ≤, in range, out of range), data index (condition =, <, >, ≥, ≤, range)
	error condition setup	RS-FEC error, out of range error, CRC error, SFD error
Decode	display type	decoded bus, tabulated list, details, decode layers
	color coding	for different cell types
	data format	hex, octal, binary, signed, unsigned
	decode layer	ternary symbols, scrambled bit, descrambled bit, corrected RS-FEC symbols
	result export	export of all result data into CSV, XML, HTML and PY file formats
Search	search event setup	frame start
		MAC frame
		idle frame
		error conditions
	event settings	same as trigger event settings

R&S®RTP-K60 USB 1.0/1.1/2.0 serial triggering and decoding

Protocol configuration	signal type	single-ended, differential
	protocol type	low, full and high speed
	bit rate	standard bit rates (1.5/12/480 Mbit/s)
	source	any input channel
	probe type	
	for low and full speed	single-ended probe
	for high speed	differential probe (R&S®RT-ZDx)
	auto threshold setup	assisted threshold configuration for USB triggering and decoding
Trigger [12]	trigger event setup	start of packet, end of packet, PID token (IN, OUT, SETUP, SOF), PID data (Data0, Data1, Data2 [11], MData [11]), PID handshake (ACK, NAK, STALL, NYET [11]), PID special (PRE[12], ERR [11], SPLIT [11], PING [11]); bus state (reset [12], resume [12], suspend [12]); error condition
	address, endpoint and frame setup SC, port, SEU, ET check (SPLIT) [12]	condition =, ≠, ≥, ≤, in range, out of range
	data setup	data pattern up to 4 byte (hex, decimal, octal, binary or ASCII), bit separately configurable (1, 0 or don't care); condition =, ≠; position based or window based triggering (first occurrence in packet payload)
	error condition	any error, PID error, CRC5 error, CRC16 error, bit stuffing error, unexpected PID, SE1 error [12] and glitching error
Decode	source	any input channel, math waveform
	display type	decoded bus, logical signal, bus + logical signal, tabulated list
	color coding	packet identifier, payload length, frame, address, endpoint, data payload, CRC5, CRC16, error condition
	data format	hexadecimal, decimal, octal, binary, ASCII, unsigned
Search	search event setup	combination of start of packet, PID token (IN, OUT, SETUP, SOF), PID data (Data0, Data1, Data2 [11], MData [11]), PID handshake (ACK, NAK, STALL, NYET [11]), PID special (PRE [12], ERR [11], SPLIT [11], PING [11]); error condition (any error, PID error, CRC5 error, CRC16 error, bit stuffing error, unexpected PID, SE1 error [12] and glitching error)
	address, endpoint and frame setup SC, port, SEU, ET check (SPLIT)	condition =, ≠, ≥, ≤, in range, out of range
	data setup	data pattern up to 4 byte (hex, decimal, octal, binary or ASCII), bit separately configurable (1, 0 or don't care); condition =, ≠; position based or window based triggering (first occurrence in packet payload)
	error condition	any error, PID error, CRC5 error, CRC16 error, bit stuffing error, unexpected PID, SE1 error [12] and glitching error

[11] Only available in high speed.

[12] Only available in low and full speed.

R&S®RTP-K61 USB 3.1 Gen 1 serial triggering and decoding

Protocol configuration	signal type	one channel
	bit rate	auto detected
	auto threshold setup	supported
	source	any analog input channels, math channels, reference channels
	scrambling	selectable
	digital signal processing	CTLE continuous time equalizer; DFE decision feedback equalizer
Trigger	trigger event setup	frame start
		frame content
		errors
	frame content	USB packet types: TSEQ, TSET1, TSET2, set link function, U2 inactivity timeout, vendor device test, port capability, port configuration, port, config. resp., link delay meas, ACK, NRDY, ERDY, STATUS, STALL, function wake, latency tolerance, bus interval, adjust, host role request, sublink speed, ping, ping response, data packet header, data packet payload, DPP aborted, isochronous timestamp, link command, info, BRST, BDAT, BERC, BCNT, idle; fields according to selected USB packet with content conditions =, ≠, <, >, ≥, ≤, in range, out of range
	errors	CRC, length, value out of range
Decode	display type	decoded bus, tabulated list, details, decode layers
	color coding	cell and frame types
	data format	hexadecimal, octal, binary, ASCII, signed, unsigned, symbols
	decode layer	edges, bit, scrambled symbols, descrambled symbols, byte
	result export	export of all result data into CSV, XML, HTML and PY file formats
Search	search event setup	frame start
		frame content
		errors
	event settings	same as trigger event settings

R&S®RTP-K62 USB 3.1 Gen 2 serial triggering and decoding

Protocol configuration	signal type	one channel
	bit rate	auto detected
	auto threshold setup	supported
	source	any analog input channels, math channels, reference channels
	scrambling	selectable
	digital signal processing	CTLE continuous time equalizer; DFE decision feedback equalizer
Trigger	trigger event setup	frame start
		frame content
		errors
	frame content	USB packet types: TSEQ, TSET1, TSET2, set link function, U2 inactivity timeout, vendor device test, port capability, port configuration, port, config. resp., link delay meas, ACK, NRDY, ERDY, STATUS, STALL, function wake, latency tolerance, bus interval, adjust, host role request, sublink speed, ping, ping response, data packet header, data packet payload, DPP aborted, isochronous timestamp, link command, info, BRST, BDAT, BERC, BCNT, idle; fields according to selected USB packet with content conditions =, ≠, <, >, ≥, ≤, in range, out of range
	errors	CRC, length, value out of range
Decode	display type	decoded bus, tabulated list, details, decode layers
	color coding	cell and frame types
	data format	hexadecimal, octal, binary, ASCII, signed, unsigned, symbols
	decode layer	edges, bit, scrambled symbols, descrambled symbols, byte
	result export	export of all result data into CSV, XML, HTML and PY file formats
Search	search event setup	frame start
		frame content
		errors
	event settings	same as trigger event settings

R&S®RTP-K63 USB power delivery serial triggering and decoding

Protocol configuration	signal type	one channel
	bit rate	auto detected
	source	any analog input channel, logical channels, math channels, reference channels
	thresholds	data, advertisements
	data details	detailed breakdown selectable
Trigger	trigger event setup	frame start
		frame content
		errors
	frame content	extended, NumDataObjs, MsgID, PwrRole/Plug, Rev, DataRole, MsgType, voltage advertisements (content conditions =, ≠, <, >, ≥, ≤, in range, out of range)
	errors	4b5b, preamble, CRC, length, SOP warning

Decode	display type	decoded bus, logical signal, bus + logical signal, tabulated list, details, decode layers
	color coding	cell and frame types
	data format	hex, octal, binary, signed, unsigned
	decode layer	edges, bit, 4b5b symbols
Search	search event setup	frame start
		frame content
		errors
	event settings	same as trigger event settings

R&S®RTP-K64 USB 3.1 SSIC serial triggering and decoding

Protocol configuration	signal type	up to 4 lanes differential
	bit rate	auto detected
	source	any analog input channels, math channels, reference channels
	scrambling	selectable
	digital signal processing	CTLE continuous time equalizer; DFE decision feedback equalizer
Trigger	trigger event setup	frame start
		frame content
		errors
	frame content	USB packet types: TSEQ, TSET1, TSET2, set link function, U2 inactivity timeout, vendor device test, port capability, port configuration, port, config. resp., link delay meas, ACK, NRDY, ERDY, STATUS, STALL, function wake, latency tolerance, bus interval, adjust, host role request, sublink speed, ping, ping response, data packet header, data packet payload, DPP aborted, isochronous timestamp, link command, info, BRST, BDAT, BERC, BCNT, idle; fields according to selected USB packet with content conditions =, ≠, <, >, ≥, ≤, in range, out of range
	errors	CRC, length, value out of range
Decode	display type	decoded bus, tabulated list, details, decode layers
	color coding	cell and frame types
	data format	hex, octal, binary, signed, unsigned
	decode layer	off, edges, bit, byte, 8b10b symbols, LCC bit, descrambler, lane merge
Search	search event setup	frame start
		frame content
		errors
	event settings	same as trigger event settings

R&S®RTP-K65 SpaceWire serial triggering and decoding

Protocol configuration	signal type	two channels: strobe and data (differential or single-ended)
	bit rate	auto adjust (strobe + data)
	source	any analog input channels, logical channels [13], math channels, reference channels
Trigger	trigger event setup	control frame, data pattern, null frame, time code, error condition
	control frame setup	any, FCT, EOP, EEP
	data pattern setup	8 bit (condition =, ≠, <, >, ≥, ≤, in range, out of range)
	time code setup	8 bit (condition =, ≠, <, >, ≥, ≤, in range, out of range)
	errors condition setup	parity, ESC
Decode	display type	decoded bus, logical signal, bus + logical signal, tabulated list, decode layers
	color coding	control frame, data frame, null frame, time code
	data format	hex, octal, binary, signed, unsigned
Search	search event setup	control frame, data pattern, null frame, time code, error
	event settings	same as trigger event settings

R&S®RTP-K72 PCI Express 1.1/2.0 serial triggering and decoding

Protocol configuration	signal type	up to four channels (×1, ×2, ×4 link size) differential signals
	bit rate	predefined 2.5 Gbit/s for Gen 1 and 5 Gbit/s for Gen 2
	source	any analog input channels, math channels, reference channels
	digital signal processing	CTLE continuous time equalizer; DFE decision feedback equalizer
Trigger	trigger event setup	TLP (transaction layer packets), DLLP (data layer packets), ordered sets, errors
	transaction layer packets (TLP)	any type, memory request (32 bit/64 bit, R/W, ordering, snoop, seq. number, Requester ID), I/O transactions, configuration requests, message requests (incl. routing and message code), completion packets (status, completer ID), atomic operation (FetchAdd, SWAP, CAS) for 32 bit/64 bit
	data layer packets (DLLP)	any type, Ack and Nak (seq. number), InitFC1, InitFC2, updateFC (credit type C, NP, Cpl and virtual channel), power management with PM type, vendor packet format. multi-root I/O virtualization (MRDLLP): MRInit (phase, VH FC, mixed type, authorized, device/port type), MRReset (A, VH Group), MRUpdateFC, MRInitFC1 and MRInitFC2 (VL number, VH absent, TLP type, credit type)
	ordered sets	SKP OS, training sequence (TS1, TS2), fast training sequence (FTS), electrical idle OS, electrical idle exit OS, compliance and modified compliance pattern
	errors condition setup	CRC16, ECRC, LCRC, disparity, invalid packets (corrupt header or length errors)

[13] SpaceWire protocol trigger on logical channels is not available.

Decode	display type	decoded bus, tabulated list, decode layers, detailed result display for packets
	color coding	TLP, DLLP, K-code, D-code, ordered sets, errors
	data format	K/D symbol, 8 bit format (hex)
	decode layer	8b10b, descrambled 8b10b, bit
	result export	export of all result data into CSV, XML, HTML and PY file formats
Search	search event setup	TLP, DLLP, ordered sets, errors
	event settings	same as trigger event settings

R&S®RTP-K73 PCI Express 3.0 serial triggering and decoding

Protocol configuration	signal type	up to four channels (×1, ×2, ×4 link size) differential signals
	bit rate	predefined 8 Gbit/s
	source	any analog input channels, math channels, reference channels
	digital signal processing	CTLE continuous time equalizer; DFE decision feedback equalizer
Trigger	trigger event setup	TLP (transaction layer packets), DLLP (data layer packets), ordered sets, errors
	transaction layer packets (TLP)	any type, memory request (32 bit/64 bit, R/W, ordering, snoop, seq. number, requester ID), I/O transactions, configuration requests, message requests (incl. routing and message code), completion packets (status, completer ID), atomic operation (FetchAdd, SWAP, CAS) for 32 bit/64 bit
	data layer packets (DLLP)	any type, Ack and Nak (seq. number), InitFC1, InitFC2, updateFC (credit type C, NP, Cpl and virtual channel), power management with PM type, vendor packet format. multi-root I/O virtualization (MRDLLP): MRInit (phase, VH FC, mixed type, authorized, device/port type), MRReset (A, VH Group), MRUpdateFC, MRInitFC1 and MRInitFC2 (VL number, VH absent, TLP type, credit type)
	ordered sets	SKP OS, training sequence (TS1, TS2), fast training sequence (FTS), electrical idle OS, electrical idle exit OS, compliance and modified compliance pattern
	errors condition setup	CRC16, ECRC, LCRC, disparity, invalid packets (corrupt header or length errors)
Decode	display type	decoded bus, tabulated list, decode layers, detailed result display for packets
	color coding	TLP, DLLP, K-code, D-code, ordered sets, errors
	data format	hex, octal, binary
	decode layer	edges, bit
	result export	export of all result data into CSV, XML, HTML and PY file formats
Search	search event setup	TLP, DLLP, ordered sets, errors
	event settings	same as trigger event settings

R&S®RTP-K81 PCI Express 1.1/2.0 compliance test

The option is used in combination with the free-of-charge R&S®ScopeSuite PC software, which can be downloaded from the Rohde & Schwarz website. R&S®RTP-K81 performs PCIe 1.x/2.0 (up to 2.5GT/s) compliance test measurements with R&S®ScopeSuite. The chapters after the category refer to PCI Express Base Specification Revision 1.1 and 2.1.

Supported PCIe compliance tests		
PCIe 1.1	signal quality (4.3.3)	mean unit interval
		data rate
		template tests
		min eye width
		median to max. jitter
		differential output voltage
	reference clock (1.32)	differential input high voltage
		differential input low voltage
		duty cycle
		average clock period
		rising edge rate
		falling edge rate
	common-mode output voltage (4.3.3)	RMS AC peak common mode output voltage
		AVG DC common mode output voltage
		DC common mode line delta
		DC common mode output voltage variation
	common-mode input voltage (4.3.3)	AC common mode input voltage
PCIe 2.0	signal quality (4.3.3)	mean unit interval
		data rate
		template tests
		min eye width
		median to max. jitter
		differential output voltage

R&S®RTP-K83 PCI Express 1.1/2.0/3.0 compliance test

The option is used in combination with the free-of-charge R&S®ScopeSuite PC software, which can be downloaded from the Rohde & Schwarz website. R&S®RTP-K83 performs PCIe 1.1/2.0/3.0 compliance test measurements with R&S®ScopeSuite.

Supported PCIe compliance tests		
PCIe 1.1	signal quality (4.3.3)	mean unit interval
		data rate
		template tests
		min. eye width
		median to max. jitter
		differential output voltage
	reference clock (1.32)	differential input high voltage
		differential input low voltage
		duty cycle
		average clock period
		rising edge rate
		falling edge rate
	common mode output voltage (4.3.3)	RMS AC peak common mode output voltage
		AVG DC common mode output voltage
		DC common mode line delta
		DC common mode output voltage variation
	common mode input voltage (4.3.3)	AC common mode input voltage
PCIe 2.0	signal quality (4.3.3)	mean unit interval
		data rate
		template tests
		min eye width
		median to max. jitter
		differential output voltage

PCIe 3.0	signal quality (4.3.3.13)	mean unit interval
		data rate
		template tests
		min. eye width
	TX base specifications (4.3.3.13.1)	TX voltage with no equalization
		min. swing during electrical idle exit sequence ordered set (EIEOS)
		pseudo package loss
		uncorrelated total jitter
		uncorrelated deterministic jitter
		uncorrelated total pulse width jitter
		uncorrelated deterministic pulse width jitter
		data dependent jitter
	reference clock (4.3.8)	REF_{CLK} frequency
		REF_{CLK} jitter
		sSsc frequency range
		ssc deviation
	common-mode output voltage (4.3.3.13)	AC common mode voltage (30 kHz to 500 MHz)
		AC common mode voltage (< 4 GHz lowpass filter)
		transmitter avg dc common mode voltage
		DC common mode voltage between d+ and d-
		DC common mode voltage during l0 and electrical idle
	TX equalization presets (4.3.3.5.2)	p0-p10 deemphasis
		p0-p10 preshoot

R&S®RTP-K87 Ethernet compliance test (1000BASE-T1)

The option is used in combination with the free-of-charge R&S®ScopeSuite PC software, which can be downloaded from the Rohde & Schwarz website. R&S®RTP-K87 performs 1000BASE-T1 compliance test measurements with R&S®ScopeSuite. R&S®ScopeSuite supports the R&S®RT-ZF6 frequency converter as well as R&S®RT-ZF7A and R&S®RT-ZF8 test fixtures. The chapters in front of the test cases refer to IEEE 802.3-2018. OPEN Alliance ECU specification supported, where applicable.

Supported 1000BASE-T1 compliance tests	
1000BASE-T1	97.5.3.3 transmitter timing jitter master mode
	97.5.3.3 transmitter timing jitter slave mode
	97.5.3.3 transmitter timing MDI jitter
	97.5.3.6 transmitter clock frequency
	97.5.3.2 transmitter distortion
	97.5.3.4 transmitter power spectral density (PSD)
	97.5.3.4 transmitter power level
	97.5.3.5 transmitter peak differential output
	97.5.3.1 maximum output droop
	97.7.2.1 MDI return loss
	97.7.2.2 MDI mode conversion loss
	MDI adapter verification

R&S®RTP-K88 Ethernet compliance test (MGBASE-T1)

The option is used in combination with the free-of-charge R&S®ScopeSuite PC software, which can be downloaded from the Rohde & Schwarz website. R&S®RTP-K88 performs MGBASE-T1 compliance test measurements with R&S®ScopeSuite. R&S®ScopeSuite supports R&S®RT-ZF7A and R&S®RT-ZF8 test fixtures. The chapters in front of the test cases refer to IEEE P802.3ch.

Supported MGBASE-T1 compliance tests	
MGBASE-T1 (2.5/5/10G)	149.5.2.1 maximum output droop
	149.5.2.2 transmitter linearity
	149.5.2.3 transmitter timing jitter master
	149.5.2.3 transmitter timing jitter slave
	149.5.2.3.1 transmit MDI random jitter in master mode
	149.5.2.3.2 transmit MDI deterministic jitter in master mode
	149.5.2.4 transmitter power spectral density (PSD) and power level
	149.5.2.5 transmitter peak differential output
	149.5.2.6 transmitter clock frequency
	149.8.2.1 MDI return loss

R&S®RTP-K89 Ethernet compliance test (10BASE-T1)

The option is used in combination with the free-of-charge R&S®ScopeSuite PC software, which can be downloaded from the Rohde & Schwarz website. R&S®RTP-K89 performs 10BASE-T1 compliance test measurements with R&S®ScopeSuite. R&S®ScopeSuite supports the R&S®RT-ZF7A and R&S®RT-ZF8 test fixtures. The chapters in front of the test cases refer to IEEE P802.3cg.

Supported 10BASE-T1 compliance tests	
10BASE-T1S	147.5.4.1 transmitter output voltage
	147.5.4.3 transmitter timing jitter
	147.5.4.2 transmitter output droop
	147.5.4.4 transmitter power spectral density (PSD)
	147.7.2 MDI return loss
	147.7.3 MDI mode conversion
10BASE-T1L	146.5.4.1 transmitter output voltage
	146.5.4.3 transmitter timing jitter
	146.5.4.5 transmitter clock frequency
	146.5.4.4 transmitter power spectral density (PSD) and power level
	146.8.3 MDI return loss
	146.8.4 MDI mode conversion

R&S®RTP-K91 DDR3/DDR3L/LPDDR3 signal integrity debug and compliance test

The option is used in combination with the free-of-charge R&S®ScopeSuite PC software, which can be downloaded from the Rohde & Schwarz website. R&S®RTP-K91 performs DDR3 (JESD79-3F), DDR3L(JESD79-3-1A.01) and LPDDR3 (JEDS209-3C) compliance test measurements with R&S®ScopeSuite. Furthermore, it enables the DDR3 decode capability to separate read and write bursts as well as the eye analysis function for mask testing on the oscilloscope.

Supported DDR3 compliance tests		
Timing tests	clock timing (12.1)	tCK(avg) (12.1.1)
		tCK(abs) (12.1.2)
		tCL(avg) (12.1.3)
		tCH(avg) (12.1.3)
		tJIT(per) (12.1.4)
		tJIT(duty) (12.1.4)
		tJIT(cc) (12.1.5)
		tERR(nper) (12.1.6)
	data timing (4.13.2, 13.4, 13.6)	tDS(base) (13.6)
		tDH(base) (13.6)
		tDS(derate) (13.6)
		tDH(derate) (13.6)
		tHZ (4.13.2)
		tLZ (4.13.2)
		tDIPW (13.4 note 28)
		tDQSQ (4.13.2)
		tQH (4.13.2)
	strobe timing (4.13, 4.14, 8.3.1)	tDQSCK (4.13.2)
		tLZ (4.13.2)
		tHZ (4.13.2)
		tRPRE (4.13.2)
		tRPST (4.13.2)
		tQSH (4.13.2)
		tQSL (4.13.2)
		tDQSS (4.14.2)
		tDQSH (4.14.2)
		tDQSL (4.14.2)
		tDSS (4.14.2)
		tDSH (4.14.2)
		tWPST (4.14.2)
		tWPRE (4.14.2)
		tDVAC (strobe) (8.3.1)
		tDVAC (clock) (8.3.1)
	command timing (13.5)	tIS (13.5)
		tIS (derated) (13.5)
		tIH (13.5)
		tIH (derated) (13.5)
		tIPW (13.5)
		tVAC (CA) (13.5)
	address timing (13.5) DDR3 and DDR3L	tIS (13.5)
		tIS (derated) (13.5)
		tIH (13.5)
		tIH (derated) (13.5)
		tIPW (13.5)
		tVAC (CA) (13.5)
	address timing (4.2) LPDDR3	tISCA (4.2)
		tIHCA (4.2)
		tIPWCA (4.2)
		tVAC (CA) (13.5)
	chip select timing (13.5) DDR3 and DDR3L	tIS (13.5)
		tIS (derated) (13.5)
		tIH (13.5)
		tIH (derated) (13.5)
		tIPW (13.5)
	chip select timing (4.2) LPDDR3	tISCS (4.2)
		tIHCS (4.2)
		tIPWCS (4.2)
		tVAC(CS) (11.5)

Electrical tests single-ended measurements	input slew rate for ADD and CMD DDR3 and DDR3L (8.5, 13.5) LPDDR3 (7.6, 11.5)	SR(tIS) rising
		SR(tIS) falling
		SR(tIH) rising
		SR(tIH) falling
	input slew rate for DQ and DM DDR3 and DDR3L (8.5, 13.6) LPDDR3 (7.6, 11.6)	SR(tIS) rising
		SR(tIS) falling
		SR(tIH) rising
		SR(tIH) falling
	AC and DC input levels for ADD and CMD DDR3(8.1.1) DDR3L(3.1) LPDDR3(7.1.1)	VIH (AC)
		VIL (AC)
		VIH (DC)
		VIL (DC)
	AC input levels for CK and DQS (8.3.3)	VSEH (AC)
		VSEL (AC)
	output slew rate for DQ (9.3)	SRQse rising
		SRQse falling
	AC and DC output levels for DQ (9.2)	VOH(AC)
		VOL(AC)
		VOH(DC)
		VOL(DC)
	AC overshoot and undershoot for ADD and CMD (9.6.1)	overshoot amplitude
		overshoot area
		undershoot amplitude
		undershoot area
	AC overshoot and undershoot for CK, DQ, DQS and DM (9.6.2)	overshoot amplitude
		overshoot area
		undershoot amplitude
		undershoot area
Electrical tests differential measurements	AC input levels for CK and DQS (8.3)	VIHdiff (AC)
		VILdiff (AC)
	AC differential cross point voltage for CK (8.4)	VIX (AC)
	differential output slew rate for DQS (9.4)	SRQdiff rising
		SRQdiff falling
	differential AC output levels for DQS (9.2)	VOHdiff(AC)
		VOLdiff(AC)
Debug	trigger write cycle	configures the oscilloscope to trigger on a write cycle
	trigger read cycle	configures the oscilloscope to trigger on a read cycle
DDR3 decoding		
Protocol configuration	signal type	DQ, DQS
	bit rate	adjustable
	threshold setup	manual threshold/hysteresis configuration
	source	analog channels
Decode	display type	decoded bus, tabulated list, details
	color coding	read frame, write frame
	data format	hex, octal, binary, signed, unsigned
	decode layer	edges, bit, words
Search	search event setup	frame content, error
	frame content	data; conditions =, ≠, <, ≤, >, ≥, in range, out of range
	error	length, frame incomplete

DDR3 eye diagram		
General description	The DDR3 eye diagram allows the user to generate eye diagrams from long multi-period acquisitions of clock signals and serial data signals. It allows the fine control of the signal content that contributes to the eye diagram and enables the advanced analysis, measurement, mask test and navigation functions.	
General configuration	number of eye diagram instances	up to 4; independently configurable
	main source	analog channels, differential channels, math channels, reference channels, track channels
	timing reference source	analog channels, differential channels, math channels, reference channels, track channels
	horizontal settings	range, position; expressed in absolute time or relative to user-defined bit rate
Display	persistence	50 ms to 50 s, or infinite
	trace colors	predefined or user-defined color tables
	eye stripe	displays position of eye diagram slices and masks violations time-correlated to the main source waveform; always enabled, for mask tests only, disabled
Qualification	gate	
	position	start, stop; absolute time or relative to display in percent
	coupling	none, cursor, zoom
	signal	
	source	analog channels, math channels, reference channels
	condition	greater than, less than, in range, out of range; relative to selected reference level
Filter	DDR3 protocol	
	frame type	any, read frame, write frame
	error	length
	bit sequence	
	mode	all, level transition, constant level, bit pattern
	bit pattern setup	up to 8 prefix bit and up to 5 suffix bit with respect to central eye diagram bit
Mask testing	mask test results	
	counters	acquisitions, slices, sample hits, slice hits, fail rate
	violation details	number and position of mask violation, expressed as time instant and slice index
	navigation and zoom	use zoom coupling to navigate to violation upon clicking the corresponding table item

R&S®RTP-K92 eMMC compliance test

The option is used in combination with the free-of-charge R&S®ScopeSuite PC software, which can be downloaded from the Rohde & Schwarz website. R&S®RTP-K92 performs eMMC (HS200, HS400) compliance test measurements with R&S®ScopeSuite.

Supported eMMC compliance tests		
HS200 (JESD84-B50)	CLK (10.5.2, 10.8.1)	bus signal levels tests (VIH, VIL)
		interface timing tests (t_{Period}, rise time, fall time, duty cycle)
	CMD push pull (10.5.2, 10.8.1)	bus signal levels tests (VIH, VIL, VOH, VOL)
		interface timing tests (setup time, hold time)
	CMD open drain (10.5.1)	bus signal levels tests (VOH, VOL)
	DAT data write (10.5.2, 10.8.1)	bus signal levels tests (VIH, VIL)
		interface timing tests (setup time, hold time)
	DAT data read (10.5.2, 10.8.1)	bus signal levels tests (VOH, VOL)
HS400 (JESD84-B50)	CLK (10.5.2, 10.10.1)	bus signal levels tests (VIH, VIL)
		interface timing tests (t_{Period}, slew rate, duty cycle distortion, minimum pulse width)
	CMD push pull (10.5.2, 10.10.1)	bus signal levels tests (VIH, VIL, VOH, VOL)
		interface timing tests (setup time, hold time)
	CMD open drain (10.5.1)	bus signal levels tests (VOH, VOL)
	DAT data write (10.5.2, 10.10.1)	bus signal levels tests (VIH, VIL)
		interface timing tests (setup time, hold time, slew rate)
	DAT data read (10.5.2, 10.10.2)	bus signal levels tests (VOH, VOL)
		interface timing tests (output skew, output hold skew, slew rate)
	data strobe for data read (10.5.2, 10.10.1)	bus signal levels tests (VOH, VOL)
		interface timing tests (t_{Period}, slew rate, duty cycle distortion, minimum pulse width)

R&S®RTP-K93 DDR4/LPDDR4 signal integrity debug and compliance test

The option is used in combination with the free-of-charge R&S®ScopeSuite PC software, which can be downloaded from the Rohde & Schwarz website. R&S®RTP-K93 performs DDR4 (JESD79-4B), LPDDR4 (JESD209-4B) and LPDDR4X(JESD209-4-1) compliance test measurements with R&S®ScopeSuite. Furthermore, it enables the DDR4 decode capability to separate read and write bursts as well as the eye analysis function for mask testing on the oscilloscope.

Supported DDR4 compliance tests		
Timing tests	clock timing (13.3)	tCK(abs) (13.3.1)
		tCK(avg) (13.3.2)
		tCL(avg) (13.3.3)
		tCH(avg) (13.3.3)
		tJIT(per) (13.3.4)
		tJIT(duty) (13.3.4)
		tJIT(cc) (13.3.4)
		tERR(nper) (13.3.4)
	data timing (4.24.1.2, 4.24.1.3)	tDQSQ (4.24.1.2)
		tQH (4.24.1.2)
		tLZ(DQ) (4.24.1.3)
		tHZ(DQ) (4.24.1.3)
	strobe timing (8.3.1, 4.24.1, 4.25.1)	tDVAC(Strobe) (8.3.1)
		tDVAC(Clock) (8.3.1)
		tLZ(DQS) (4.24.1)
		tHZ(DQS (4.24.1)
		tDQSCK (4.24.1)
		tRPRE (4.24.1)
		tRPST (4.24.1)
		tQSH (4.24.1)
		tQSL (4.24.1)
		tDQSS (4.25.1)
		tDQSH (4.25.1)
		tDQSL (4.25.1)
		tDSS (4.25.1)
		tDSH (4.25.1)
		tWPRE (4.25.1)
	command timing (13.7)	tIS(base) (13.7)
		tIH(base) (13.7)
		tIPW (13.7)
	address timing (13.7)	tIS(base) (13.7)
		tIH(base) (13.7)
		tIPW (13.7)
	chip select timing (13.7)	tIS(base) (13.7)
		tIH(base) (13.7)
		tIPW (13.7)

Electrical tests single-ended measurements	AC and DC input levels for ADD and CMD (8.1)	VIH(AC)
		VIL(AC)
		VIH(DC)
		VIL(DC)
	AC input levels for CK (8.3.3)	VSEH(AC)
		VSEL(AC)
	AC overshoot and undershoot for ADD, CMD (8.3.4)	VAOSP
		VAOS
		VAUS
		AAOS2
		AAOS1
		AAUS
	AC overshoot and undershoot for CK (8.3.5)	VCOSP
		VCOS
		VCUS
		ACOS2
		ACOS1
		ACUS
	AC overshoot and undershoot for DQ, DQS and DM (8.3.6)	VDOSP
		VDOS
		VDUS
		VDUSP
		ADOS2
		ADOS1
		ADUS1
		ADUS2
	input slew rate for ADD and CMD (8.4.2)	SR(tIS) rising
		SR(tIS) falling
		SR(tIH) rising
		SR(tIH) falling
	AC & DC output levels for DQ (9.2)	VOH(AC)
		VOL(AC)
		VOH(DC)
		VOL(DC)
	output slew rate for DQ (9.4)	SRQse rising
		SRQse falling
Electrical tests differential measurements	AC and DC input levels for CK (8.3.2)	VIHdiff(AC)
		VILdiff(AC)
		VIHdiff(DC)
		VILdiff(DC)
	input slew rate for CK (8.4.1)	SRdiff rising
		SRdiff falling
	differential cross point voltage for CK (8.5)	VIX(CK)
	AC input levels for DQS (8.7.2)	VIHDiffPeak
		VILDiffPeak
	input slew rate for DQS (8.7.5)	SRdiff rising
		SRdiff falling
	differential AC output levels for DQS (9.3)	VOHdiff(AC)
		VOLdiff(AC)
	differential output slew rate for DQS (9.5)	SRQdiff rising
		SQQdiff falling
DDR4 decoding		
Protocol configuration	signal type	DQ, DQS
	bit rate	adjustable
	threshold setup	manual threshold/hysteresis configuration
	source	analog channels
Decode	display type	decoded bus, tabulated list, details
	color coding	read frame, write frame
	data format	hex, octal, binary, signed, unsigned
	decode layer	edges, bit, words
Search	search event setup	frame content, error
	frame content	data; conditions =, ≠, <, ≤, >, ≥, in range, out of range
	error	length, frame incomplete

DDR4 eye diagram		
General description	The DDR4 eye diagram allows the user to generate eye diagrams from long multi-period acquisitions of clock signals and serial data signals. It allows the fine control of the signal content that contributes to the eye diagram and enables the advanced analysis, measurement, mask test and navigation functions.	
General configuration	number of eye diagram instances	up to 4; independently configurable
	main source	analog channels, differential channels, math channels, reference channels, track channels
	timing reference source	analog channels, differential channels, math channels, reference channels, track channels
	horizontal settings	range, position; expressed in absolute time or relative to user-defined bit rate
Display	persistence	50 ms to 50 s, or infinite
	trace colors	predefined or user-defined color tables
	eye stripe	displays position of eye diagram slices and masks violations time-correlated to the main source waveform; always enabled, for mask tests only, disabled
Qualification	gate	
	position	start, stop; absolute time or relative to display in percent
	coupling	none, cursor, zoom
	signal	
	source	analog channels, math channels, reference channels
	condition	greater than, less than; relative to selected reference level
Filter	DDR4 protocol	
	frame type	any, read frame, non-consecutive read frame, write frame, non-consecutive write frame
	error	length
	bit sequence	
	mode	all, level transition, constant level, bit pattern
	bit pattern setup	up to 8 prefix bit and up to 5 suffix bit with respect to central eye diagram bit
Mask testing	mask test results	
	counters	acquisitions, slices, sample hits, slice hits, fail rate
	violation details	number and position of mask violation, expressed as time instant and slice index
	navigation and zoom	use zoom coupling to navigate to violation upon clicking the corresponding table item

R&S®RTP-K94 DDR5 signal integrity debugging and compliance test

The option is used in combination with the free-of-charge R&S®ScopeSuite PC software, which can be downloaded from the Rohde & Schwarz website. R&S®RTP-K94 performs DDR5 (JESD79-5B_v1.20) compliance test measurements with R&S®ScopeSuite.

Supported DDR5 compliance tests		
Timing tests	strobe timing (4.4.3)	tWPRE2
		tWPRE3
		tWPRE4
		tWPST0.5
		tWPST1.5
		tDQSL2PRE
		tDQSL3PRE
		tDQSL4PRE
		tDQSH_pre
		tDQSL_pre
	command address timing (8.2)	VciVW
		TcIVW
		VIHL_AC
		TcIPW
		SRIN_cIVW
	clock timing (8.3.2)	tCK
		tCK_Duty_UI_Error
		tCK_1UI_Rj_NoBUJ
		tCK_1UI_Dj_NoBUJ
		tCK_1UI_Tj_NoBUJ
Input levels tests	differential input voltage for CK (8.5.2)	VIHdiff(CK)
		VILdiff(CK)
	differential input voltage for DQS (8.9.3)	VIHdiff(DQS)
		VILdiff(DQS)
	differential input slew rate for CK (8.5.3)	SRIdiff rising
		SRIdiff falling
	differential input slew rate for DQS (8.9.4)	SRIdiff rising
		SRIdiff falling
	differential input cross point voltage for CK (8.4)	VIX_CK_Ratio
	differential input cross point voltage for DQS (8.8)	VIX_DQS_Ratio
Output levels tests	differential AC output levels for DQS (9.7)	VOHdiff(AC)
		VOLdiff(AC)
	differential output slew rate for DQS (9.8)	SRQdiff rising
		SRQdiff falling
Overshoot/undershoot	AC overshoot and undershoot for CK	VCOSP
		VCOS
		VCUS
		ACOS2
		ACOS1
		ACUS
DDR5 decoding		
Protocol configuration	signal type	DQ, DQS, CA4, CS
	bit rate	adjustable
	read settings	read CAS latency, read preamble type
	write settings	write CAS latency, write preamble type
	threshold setup	manual threshold/hysteresis configuration
	source	analog channels
Decode	display type	decoded bus, tabulated list, details
	color coding	read frame, write frame
	data format	hex, octal, binary, signed, unsigned
	decode layer	edges, bit, words
Search	search event setup	frame content, error
	frame content	data; conditions =, ≠, <, ≤, >, ≥, in range, out of range
	error	length, frame incomplete

DDR5 eye diagram		
General description	The DDR5 eye diagram allows the user to generate eye diagrams from long multiperiod acquisitions of clock signals and serial data signals. It allows the fine control of the signal content that contributes to the eye diagram and enables the advanced analysis, measurement, mask test and navigation functions.	
General configuration	number of eye diagram instances	up to 4; independently configurable
	main source	analog channels, differential channels, math channels, reference channels, track channels
	timing reference source	analog channels, differential channels, math channels, reference channels, track channels
	horizontal settings	range, position; expressed in absolute time or relative to user-defined bit rate
Display	persistence	50 ms to 50 s, or infinite
	trace colors	predefined or user-defined color tables
	eye stripe	displays position of eye diagram slices and masks violations time-correlated to the main source waveform; always enabled, for mask tests only, disabled
Qualification	gate	
	position	start, stop; absolute time or relative to display in percent
	coupling	none, cursor, zoom
	signal	
	source	analog channels, math channels, reference channels
	condition	greater than, less than; relative to selected reference level
Filter	DDR5 protocol	
	frame type	any, read frame, non-consecutive read frame, write frame, non-consecutive write frame
	error	length
	bit sequence	
	mode	all, level transition, constant level, bit pattern
	bit pattern setup	up to 8 prefix bit and up to 5 suffix bit with respect to central eye diagram bit
Mask testing	mask test results	
	counters	acquisitions, slices, sample hits, slice hits, fail rate
	violation details	number and position of mask violation, expressed as time instant and slice index
	navigation and zoom	use zoom coupling to navigate to violation upon clicking the corresponding table item

R&S®RTP-K95 LPDDR5 signal integrity debugging and compliance test

The option is used in combination with the free-of-charge R&S®ScopeSuite PC software, which can be downloaded from the Rohde & Schwarz website. R&S®RTP-K95 performs LPDDR5 (JESD209-5C) compliance test measurements with R&S®ScopeSuite.

Supported LPDDR5/LPDDR5X compliance tests		
Timing tests	differential clock timing (15.1)	tCK(avg)
		tCH(avg)
		tCL(avg)
		tCK(abs)
		tCH(abs)
		tCL(abs)
		tJIT(per)
		tJIT(cc)
	differential write clock timing (15.2)	tWCK(avg)
		tWCH(avg)
		tWCL(avg)
		tWCK(abs)
		tWCH(abs)
		tWCL(abs)
		tJIT(per)_WCK
		tJIT(cc)_WCK
		tERR(nper)_WCK
	WCK to CK phase offset (4.2.5)	tWCK2CK
	single-ended clock timing (12.6)	tCKHL
		tCKH
		tCKL
	single-ended write clock timing (12.5)	tWCKHL
		tWCKH
		tWCKL
	write DQ timing (15.7)	tDIHL
		tDIPW1
		tDIPW2
Eye diagram tests	CS RX mask testing (15.5)	tCSIVW1 margin
		tCSIVW2 margin
		vCSIVW margin
		tCSIPW
		CS VIHL(ac)
	CA RX mask test (15.6)	tCIVW1 margin
		tCIVW2 margin
		vCIVW margin
		tCIPW
		CA VIHL(ac)
	DQ RX mask test (15.7)	tDIVW1 margin
		tDIVW2 margin
		vDIVW margin
		tDIPW
		DQ VIHL(ac)
Input levels tests	differential input peak voltage for CK (12.2.1)	Vindiff_CK
	differential input peak voltage for WCK (12.2.2)	Vindiff_WCK
	differential input voltage for CK (12.2.1.3)	VIHdiff_CK
		VIHdiff_CK
	differential input voltage for WCK (12.2.2.3)	VIHdiff_WCK
		VILdiff_WCK
	differential input slew rate for CK (12.2.1.3)	SRIdiff_CK rising
		SRIdiff_CK falling
	differential input slew rate for WCK (12.2.2.3)	SRIdiff_WCK rising
		SRIdiff_WCK falling
	differential input cross point voltage for CK (12.2.1.4)	Vix_CK_ratio
	differential input cross point voltage for WCK (12.2.2.4)	Vix_WCK_ratio
	single-ended input voltage for CK (12.2.1.2)	Vinse_CK
		Vinse_CK_High
		Vinse_CK_Low

	single-ended input voltage for WCK (12.2.2.2)	Vinse_WCK
		Vinse_WCK_High
		Vinse_WCK_Low
	single-ended mode input voltage for CK (12.6.2)	Vinse_CK_SE
		Vinse_CK_SE_High
		Vinse_CK_SE_Low
	single-ended mode input voltage for WCK (12.5.2)	Vinse_WCK_SE
		Vinse_WCK_SE_High
		Vinse_WCK_SE_Low
	single-ended mode input slew rate for CK (12.6.2)	SRICKSE rising
		SRICKSE falling
	single-ended mode input slew rate for WCK (12.5.2)	SRIWCKSE rising
		SRIWCKSE falling
	AC overshoot and undershoot for CK (12.1.3.1)	overshoot amplitude
		undershoot amplitude
		overshoot area
		undershoot area
	AC overshoot and undershoot for WCK (12.1.3.1)	overshoot amplitude
		undershoot amplitude
		overshoot area
		undershoot area
	AC overshoot and undershoot for DQ (12.1.3.1)	overshoot amplitude
		undershoot amplitude
		overshoot area
		undershoot area
	AC overshoot and undershoot for CA (12.1.3.1)	overshoot amplitude
		undershoot amplitude
		overshoot area
		undershoot area
	AC overshoot and undershoot for CS (12.1.3.1)	overshoot amplitude
		undershoot amplitude
		overshoot area
		undershoot area
	AC overshoot and undershoot for RDQS (12.1.3.1)	overshoot amplitude
		undershoot amplitude
		overshoot area
		undershoot area
LPDDR5 decoding		
Protocol configuration	signal type	DQ, WCK, RDQS
	bit rate	adjustable
	threshold setup	manual/auto threshold, manual hysteresis configuration
	source	analog channels, math channels, reference channels
Decode	display type	decoded write frames, tabulated list, details
	color coding	write frame
	data format	hex, octal, binary, signed, unsigned
	decode layer	edges, bit, words
Search	search event setup	frame content, error
	frame content	data; conditions =, ≠, <, ≤, >, ≥, in range, out of range
	error	length, frame incomplete
LPDDR5 eye diagram		
General description	The LPDDR5 eye diagram allows the user to generate eye diagrams from long multiperiod acquisitions of clock signals and serial data signals. It allows the fine control of the signal content that contributes to the eye diagram and enables the advanced analysis, measurement, mask test and navigation functions.	
General configuration	number of eye diagram instances	up to 4; independently configurable
	main source	analog channels, differential channels, math channels, reference channels, track channels
	timing reference source	analog channels, differential channels, math channels, reference channels, track channels
	horizontal settings	range, position; expressed in absolute time or relative to user-defined bit rate

Display	persistence	50 ms to 50 s, or infinite
	trace colors	predefined or user-defined color tables
	eye stripe	displays position of eye diagram slices and masks violations time-correlated to the main source waveform; always enabled, for mask tests only, disabled
Qualification	gate	
	position	start, stop; absolute time or relative to display in percent
	coupling	none, cursor, zoom
	signal	
	source	analog channels, math channels, reference channels
	condition	greater than, less than; relative to selected reference level
Filter	LPDDR5 protocol	
	frame type	write frame
	bit sequence	
	mode	all, level transition, constant level, bit pattern
	bit pattern setup	up to 8 prefix bit and up to 5 suffix bit with respect to central eye diagram bit
Mask testing	mask test results	
	counters	acquisitions, slices, sample hits, slice hits, fail rate
	violation details	number and position of mask violation, expressed as time instant and slice index
	navigation and zoom	use zoom coupling to navigate to violation upon clicking the corresponding table item

R&S®RTP-K98 modulated load pull

The option is used in combination with the free-of-charge R&S®ScopeSuite PC software, which can be downloaded from the Rohde & Schwarz website. R&S®RTP-K98 performs modulated load pulling in combination with an R&S®SMW200A.

General		
Frequency range		up to 8 GHz (includes IF deviation)
Load pull bandwidth		2 GHz (depending on the center frequency)
Synthesized impedance gamma (Γ) error	RMS (peak), for abs(Γ) < 1	0.02 Γ (0.05 Γ) (meas.)
Convergence time		10 s (meas.), with stable reflection coefficient, ready to measure; dependent on the DUT and PC hardware
Load pull gamma range		unlimited, depends on usage of additional lab amplifier
R&S®SMW200A power output (depending on R&S®SMW200A model and frequency)	average power	18 dBm
	peak envelope power (max.)	30 dBm
R&S®RTP power input	peak envelope power (linear operation)	0 dBm
	peak envelope power (max.)	24 dBm
API automation	language	Python, C#
Specialized features		envelope tracking support
Requirements		
Oscilloscope	R&S®RTP084B, R&S®RTP134B or R&S®RTP164B	R&S®RTP oscilloscope with ≥ 8 GHz bandwidth
	R&S®RTP-K11	I/Q software interface
	2 × RT-ZA16	precision BNC to SMA adapter
Vector signal generator	R&S®SMW200A	base unit
	R&S®SMW-B1007 or higher	100 kHz to 7.5 GHz, path A
	R&S®SMW-B2007 or higher	100 kHz to 7.5 GHz, path B
	R&S®SMW-B90	phase coherence
	R&S®SMW-B13XT	wideband, two I/Q paths to RF section
	2 × R&S®SMW-B9	wideband baseband generator, 500 MHz
	2 × R&S®SMW-K525	baseband extension 1 GHz
	2 × R&S®SMW-K527	baseband extension 2 GHz
Calibration kit	R&S®ZN-Z129	calibration kit, 2.92 mm, female; depends on the cables used

Accessory	2 × directional couplers	
	6 × SMA cables	high quality is recommended
	3 × circulators	optional if isolation is provided otherwise

R&S®RTP-K99 R&S®ScopeSuite automation

The option is used in combination with the free-of-charge R&S®ScopeSuite PC software, which can be downloaded from the Rohde & Schwarz website. It requires matching compliance test options (see below). R&S®RTP-K99 makes it possible to automate the supported compliance options remotely. After remote execution of a test case the user can collect the results to process them in a proprietary software to create own reports.

Remote API to execute test cases of R&S®ScopeSuite		
API language		C#
Supported options	R&S®RTP-K22	100BASE-TX, 1000BASE-T
	R&S®RTP-K23	2.5GBASE-T, 5GBASE-T, 10GBASE-T
	R&S®RTP-K24	100BASE-T1
	R&S®RTP-K87	1000BASE-T1
	R&S®RTP-K88	MultiGBASE-T1 (2.5G/5G/10G)
	R&S®RTP-K89	10BASE-T1L, 10BASE-T1S
	R&S®RTP-K91	DDR3, DDR3L, LPDDR3
	R&S®RTP-K92	HS200, HS400
	R&S®RTP-K93	DDR4, LPDDR4, LPDDR4X

R&S®RTP-K101 USB 3.2 transmitter compliance test

The option is used in combination with the free-of-charge R&S®ScopeSuite PC software, which can be downloaded from the Rohde & Schwarz website. R&S®RTP-K101 performs USB 2.0/3.2 compliance test measurements with R&S®ScopeSuite.

Supported USB 3.2 compliance tests		
USB 2.0 device test	high speed	signal quality (EL_2, 4, 5, 6, 7); packet parameters (EL_21, 22, 25); chirp timing (EL_28, 29, 31); suspend/resume/reset timing (EL_27, 28, 38, 39, 40); test J/K, SE0_NAK (EL_8, 9); receiver sensitivity (EL_16, 17, 18)
	full speed and low speed	full speed signal quality; back voltage; inrush current
USB 2.0 host test	high speed	signal quality (EL_2, 3, 6, 7); packet parameters (EL_21, 22, 23, 25, 55); chirp timing (EL_33, 34, 35); suspend/resume/reset timing (EL_39, 41); test J/K, SE0_NAK (EL_8, 9)
	full speed and low speed	low speed signal quality downstream; full speed signal quality downstream; drop; droop
USB 2.0 hub test	high speed	signal quality upstream (EL_2, 4, 6, 7); signal quality downstream (EL_2, 3, 6, 7); jitter downstream (EL_47); packet parameters upstream (EL_21, 22, 25); hub receiver sensitivity upstream (EL_16, 17, 18); repeater downstream (EL_42, 43, 44, 45, 48); repeater upstream (EL_42, 43, 44, 45); chirp timing upstream (EL_28, 29, 31); suspend/resume/reset timing upstream (EL_27, 28, 38, 39, 40); test J/K, SE0_NAK upstream (EL_8, 9); test J/K, SE0_NAK downstream (EL_8, 9)
	full speed and low speed	low speed signal quality downstream; full speed signal quality upstream; full speed signal quality downstream; inrush current upstream; drop downstream; droop downstream; back voltage

USB 3.2 device test	SuperSpeed (Gen 1)	TD 1.1: low frequency periodic signaling TX; TD 1.3: long channel transmitted eye; TD 1.3: short channel transmitted eye; TD 1.6: SSC profile
	SuperSpeedPlus (Gen 2)	TD 1.4: long channel transmitted eye; TD 1.4: short channel transmitted eye; TD 1.5: transmit equalization; TD 1.7: SSC profile
USB 3.2 host test	SuperSpeed (Gen 1)	TD 1.1: low frequency periodic signaling TX; TD 1.3: long channel transmitted eye; TD 1.3: short channel transmitted eye; TD 1.6: SSC profile
	SuperSpeedPlus (Gen 2)	TD 1.4: long channel transmitted eye; TD 1.4: short channel transmitted eye; TD 1.5: transmit equalization; TD 1.7: SSC profile
USB 3.2 hub test	SuperSpeed (Gen 1)	TD 1.1: upstream low frequency periodic signaling TX; TD 1.3: upstream long channel transmitted eye; TD 1.3: upstream short channel transmitted eye; TD 1.6: upstream SSC profile; TD 1.1: downstream low frequency periodic signaling TX; TD 1.3: downstream long channel transmitted eye; TD 1.3: downstream short channel transmitted eye; TD 1.6: downstream SSC profile
	SuperSpeedPlus (Gen 2)	TD 1.4: upstream long channel transmitted eye; TD 1.4: upstream short channel transmitted eye; TD 1.5: upstream transmit equalization; TD 1.7: upstream SSC profile; TD 1.4: downstream long channel transmitted eye; TD 1.4: downstream short channel transmitted eye; TD 1.5: downstream transmit equalization; TD 1.7: downstream SSC profile

R&S®RTP-K102 USB 3.2 receiver compliance test

The option is used in combination with the free-of-charge R&S®ScopeSuite PC software, which can be downloaded from the Rohde & Schwarz website. R&S®RTP-K102 performs USB 3.2 receiver compliance test measurements with R&S®ScopeSuite. The option requires an Anritsu MP1900A signal quality analyzer (BERT) with min. 21 Gbps and equipped with the following options: synthesizer (MU181000B), SI PPG (MU195020A), SI ED (MU195040A), jitter modulation source (MU181500B), noise generator (MU195050A) and MX183000A software with USB link training.

Supported USB 3.2 receiver compliance tests		
Calibration	USB 3.2 Gen 1: 5 GT/s (Std-A, Std-B, µB)	TD.1.8.1 calibrate swing and deemphasis; TD.1.8.2 Rj Sj and eye height calibration
	USB 3.2 Gen 1: 5 GT/s (Type-C)	TD.1.9.1 calibrate swing and deemphasis; TD.1.9.2 calibrate Rj and Sj
	USB 3.2 Gen 2: 10 GT/s (Std-A, µB, Type-C)	TD.1.10.1 calibrate swing and deemphasis; TD.1.10.2 calibrate Rj; TD.1.10.3 calibrate Sj; TD.1.10.4-8 load board analysis; TD.1.10.9-11 eye height calibration
Device/Hub/Host	USB 3.2 Gen 1 jitter tolerance in loopback mode	TD.1.8/1.9.3-19 measured with sinusoidal jitter at: 33/20/10/4.9/2/1 MHz, 500 kHz
	USB 3.2 Gen 2 jitter tolerance in loopback mode	TD.1.10.14-29 measured with sinusoidal jitter at: 50/30/15/7.5/4/2/1 MHz, 500 kHz

R&S®RTP-K110 HDMI 1.4/2.1 TMDS compliance test

The option is used in combination with the free-of-charge R&S®ScopeSuite PC software, which can be downloaded from the Rohde & Schwarz website. R&S®RTP-K110 performs HDMI 1.4b/2.1 TMDS transmitter compliance test measurements with R&S®ScopeSuite.

Supported HDMI compliance tests		
HDMI 1.4b clock	all clock tests	V_I+, V_I– (7-2)
		rise/fall time (7-4)
		intra pair skew (7-7)
		duty cycle min./max. (7-8)
		jitter (7-9)
	voltage off tests	V_{off} +, V_{off} – (7-3)
HDMI 1.4b data	single-ended tests	V_I+, V_I– (7-2)
		intra pair skew (7-7)
	voltage off tests	V_{off} +, V_{off} – (7-3)
	differential timing tests	rise/fall time (7-4)
	jitter mask tests	differential voltage mask (7-10)
		jitter (7-10)
	inter-pair skew	inter pair skew (7-6)
HDMI 2.1 TMDS clock	all clock tests	V_I+, V_I– (HF 1-1)
		V_{swing} +, V_{swing} – (HF 1-1)
		rise/fall time (HF 1-2)
		intra pair skew (HF 1-4)
		duty cycle min./max. (HF 1-6)
		rate (HF 1-6)
		V_{swing} TP1 (HF 1-7)
		jitter worst case pos./neg. skew (HF 1-7)
HDMI 2.1 TMDS data	single-ended tests	V_I+, V_I– (HF 1-1)
		V_{swing} +, V_{swing} – (HF 1-1)
		intra pair skew (HF 1-4)
	differential timing tests	rise/fall time (HF 1-2)
	differential voltage mask tests	max./min. differential voltage (HF 1-5)
	jitter mask tests	mask test worst case pos./neg. skew (HF 1-8)
	inter-pair skew	inter-pair skew (HF 1-3)

Requirements		
Options	R&S®RTP-K136 (max. 8 Gbps) or R&S®RTP-K137 (max. 16 Gbps) or R&S®RTP-SIBDL2 or R&S®RTP-ALLSI	advanced eye analysis signal integrity bundles (contain the R&S®RTP-K137 16 Gbps advanced eye analysis option)
	R&S®RTP-K140 (max. 8 Gbps) or R&S®RTP-K141 (max. 16 Gbps) or R&S®RTP-SIBDL1 or R&S®RTP-ALLSI	high speed serial pattern trigger signal integrity bundles (contain the R&S®RTP-K141 16 Gbps high speed serial pattern option)

R&S®RTP-K114 DisplayPort (DP) 1.4a compliance test

The option is used in combination with the free-of-charge R&S®ScopeSuite PC software, which can be downloaded from the Rohde & Schwarz website. R&S®RTP-K114 performs DisplayPort v1.4a compliance test measurements with R&S®ScopeSuite. The numbers in front of the test refer to the DisplayPort v1.4a CTS.

Supported DisplayPort v1.4a compliance tests		
DisplayPort v1.4a	main-link tests	3.1 eye diagram tests
		3.2 HBR/RBR non-PE level verification test
		3.3 HBR/RBR level verification and peak to peak differential voltage test
		3.4 HBR3/HBR2 level verification test
		3.5 HBR3/HBR2 peak to peak differential voltage test
		3.6 inter-pair skew test
		3.7 intra-pair skew test
		3.8 AC common mode noise test
		3.9 non-ISI jitter measurement tests
		3.10 HBR3 TX differential RL test
		3.11 TJ/RJ/DJ measurement test
		3.12 main-link frequency compliance test
		3.13 spread-spectrum modulation frequency test
		3.14 spread-spectrum modulation deviation test
		3.15 dF/dT spread-spectrum deviation high-frequency variation test
	AUX CH tests	9.1 AUX_CH (Manchester-II) eye test
		9.2 AUX_CH (Manchester-II) sensitivity test
		9.3 AUX_CH_N termination DC test
		9.4 AUX_CH_P termination DC test
		9.5 AUX_CH slew rate test
	DP_PWR tests	9.6 inrush (Informative) and outrush (Informative) test
Requirements		
Options	R&S®RTP-K133	advanced jitter analysis
	R&S®RTP-K136 (max. 8 Gbps) or R&S®RTP-K137 (max. 16 Gbps)	advanced eye analysis
	R&S®RTP-K140 (max. 8 Gbps) or R&S®RTP-K141 (max. 16 Gbps) or	high speed serial pattern trigger
	alternatively: R&S®RTP-SIBDL1	signal integrity bundle (contains the R&S®RTP-K141 16 Gbps high speed serial pattern option)

R&S®RTP-K115 Embedded DisplayPort (eDP) v1.4b/1.5 compliance test

The option is used in combination with the free-of-charge R&S®ScopeSuite PC software, which can be downloaded from the Rohde & Schwarz website. R&S®RTP-K114 performs Embedded DisplayPort v1.4b/1.5 compliance test measurements with R&S®ScopeSuite.

Supported Embedded DisplayPort v1.4b and 1.5 compliance tests		
Embedded DisplayPort v1.4b and v1.5	main-link tests	eye diagram test
		jitter tests – non-ISI jitter
		jitter tests – total jitter
		jitter tests – random jitter
		jitter tests – deterministic jitter
		differential voltage test
		main-link frequency compliance test
		SSC tests – modulation frequency
		SSC tests – modulation deviation
		SSC tests – dF/dT spread-spectrum deviation high-frequency variation
		intra-pair tests – AC common mode noise
		intra-pair tests – intra-pair skew
		intra-pair tests – rise and fall time mismatch
		inter-pair skew test
	AUX CH tests	eye tests – mask test
		eye tests – peak to peak voltage
		eye tests – mask test
		sensitivity test
Requirements		
Options	R&S®RTP-K133	advanced jitter analysis
	R&S®RTP-K136 (max. 8 Gbps) or R&S®RTP-K137 (max. 16 Gbps)	advanced eye analysis

R&S®RTP-K121 deembedding base option

General description	The R&S®RTP-K121 deembedding base option allows waveform correction based on S-parameters of the involved measurement blocks. The correction parameters of a cable or a modified probe can also be determined by using proven cable/proven probe.	
Source		channel 1, channel 2, channel 3, channel 4,
Signal types		single-ended signals
		differential signals based on two separate cables by using two channels
		full differential signals based on differential probes
S-parameter files		s2p-files and s4p-files
Types of blocks		cables, connectors, fixtures and customer defined blocks
Maximum number of blocks		10

Proven cable/proven probe

General description	Proven probe/cable is a part of the R&S®RTP-K121 deembedding base option. This function enables the user to determine the correction parameters of a cable or a modified probe based on the R&S®RTP-B7 differential pulse source.	
Mode		proven cable, proven probe (Rohde & Schwarz probes, user-defined)
Configurations	proven cable	single ended
	proven probe	single ended, differential
Correction method	cable, user-defined probe	transmission (magnitude and phase)
	Rohde & Schwarz probe	transmission (magnitude and phase)
Maximal group delay of DUT		20 ns
Maximal length of cables (setup)		3 m
Source		step with amplitude of –200 mV

R&S®RTP-K122 realtime deembedding extension

General description	The R&S®RTP-K122 realtime deembedding extension option allows waveform correction based on S-parameters in realtime. This option is an extension to the R&S®RTP-K121 deembedding base option. For details, see R&S®RTP-K121 option.	
Realtime waveform acquisition rate		see acquisition system

R&S®RTP-K126 embedding and equalization option

General description	The R&S®RTP-K126 option consists of equalization (used to compensate for transmission losses and to re-open the data eye) and embedding (provides users with the capability to emulate additional signal channel components (e.g.: longer cables)).	
Lane configuration	number of lane instances	up to 4; independently configurable
	main source	analog channels, differential channels, math channels, reference channels
	vertical settings	scale, offset, position
Embedding	signal types	single ended, full differential
	S-parameter files	s2p-files and s4p-files
	block types	cables, adapters, fixtures, proven cable, and customer defined blocks
	maximum number of blocks	5
Equalization	transmission feed forward equalizer (TxFFE)	
	presets	predefined presets (dependent on the selected serial standard)
	filter taps	up to 4 taps
	continuous time linear equalizer (CTLE)	
	presets	predefined presets (dependent on the selected serial standard)
	DC gain	desired DC gain in dB
	zero frequencies	up to 6 zeros
	pole frequencies	up to 6 poles
	feed forward equalizer (FFE)	
	filter taps	up to 40 taps
	taps per symbol	track data rate, manual
	decision feedback equalizer (DFE)	
	timing reference	clock, CDR
	clock source	analog channels, differential channels, math channels, reference channels
	CDR	
	type	software
	sampling time	0.0 to 1.0 UI
	filter taps	up to 5 taps
	gain	desired gain [scalar]
	FFE and DFE training	
	mode	main source, reference waveform
	filter	FFE, FFE and DFE
	FFE	
	taps	up to 40 taps
	precursor taps	up to 39 taps
	taps per symbol	track data rate, manual
	DFE	
	taps	up to 5 taps
	tap lower limit	–1.0 to 1.0
	tap upper limit	–1.0 to 1.0
	normalize gain	filter taps will be trained to achieve a normalized gain

R&S®RTP-K130 TDR/TDT analysis

Time domain reflexion/time domain transmission analysis option		
General description	The R&S®RTP-K130 TDR/TDT option is a measurement technique used to determine the characteristics of electrical lines by observing reflected and/or transmitted waveforms. Together, they provide a powerful means of analyzing electrical transmission media.	
Mode		TDR, TDT, TDR/TDT
Configuration		single ended, full differential
Signals		impedance/reflection coefficient

Domain		time/distance
Bandwidth	TDR and/or TDT, single ended	
	R&S®RTP044B	4 GHz
	R&S®RTP064B	6 GHz
	R&S®RTP084B	8 GHz
	R&S®RTP134B	13 GHz
	R&S®RTP164B	16 GHz
	TDR or TDT, differential	
	R&S®RTP044B	4 GHz
	R&S®RTP064B	6 GHz
	R&S®RTP084B	8 GHz
	R&S®RTP134B	13 GHz
	R&S®RTP164B	16 GHz
	TDR and TDT, differential	
	R&S®RTP044B	4 GHz
	R&S®RTP064B	6 GHz
	R&S®RTP084B	8 GHz
	R&S®RTP134B	8 GHz
	R&S®RTP164B	8 GHz
Step amplitude		200 mV
Repetition rate		50 Hz to 500 kHz (depends on horizontal scale)
Length of cable	max.	15 ns (~ 3.2 m at ε_r = 2)
	min.	2 ns (~ 0.4 m at ε_r = 2)
Electrical length of short	range, adjustable by user	0 ns to 2 ns
Reference impedance	single ended	50 Ω
	differential	100 Ω

R&S®RTP-K133 advanced jitter analysis

General description	The R&S®RTP-K133 option provides advanced jitter measurements and enables jitter separation. R&S®RTP-K133 option includes R&S®RTP-K12 option.	
Jitter separation	total jitter (TJ), deterministic jitter (DJ), data dependent jitter (DDJ), periodic jitter (PJ), data dependent jitter plus periodic jitter (DDJ+PJ), random jitter (RJ), (other) bounded uncorrelated jitter ((O)BUJ), random jitter plus (other) bounded uncorrelated jitter (RJ+(O)BUJ)	
Accepted input signals	clock signals or data signals (NRZ)	
Reference clock	internal clock recovery (PLL first or second order, constant clock or feed forward) or explicit clock signal	
Basic measurements	symbol rate, symbol duration, event count	
Jitter measurements	total jitter at bit error rate (TJ@BER)	value in seconds or unit interval BER value selectable between 10^{-32} and 10^{-1}
	deterministic jitter (DJ, dual-dirac)	value in seconds or unit interval
	duty cycle distortion (DCD)	value in seconds or unit interval
	inter symbol interference (ISI)	value in seconds or unit interval
	total jitter (TJ) corresponds to time interval error (TIE)	peak-to-peak value and RMS value in seconds or unit interval
	deterministic jitter (DJ)	peak-to-peak value and RMS value in seconds or unit interval
	data dependent jitter (DDJ)	peak-to-peak value and RMS value in seconds or unit interval
	periodic jitter (PJ)	peak-to-peak value and RMS value in seconds or unit interval
	data dependent jitter plus periodic jitter (DDJ+PJ)	peak-to-peak value and RMS value in seconds or unit interval
	periodic jitter components	amplitude, frequency, direction (vertical or horizontal)
	random jitter (RJ)	RMS value in seconds or unit interval
	(other) bounded uncorrelated jitter ((O)BUJ)	peak-to-peak value and RMS value in seconds or unit interval
	(other) bounded uncorrelated jitter ((O)BUJ, dual-dirac)	value in seconds or unit interval
	random jitter plus (other) bounded uncorrelated jitter (RJ+(O)BUJ)	peak-to-peak value and RMS value in seconds or unit interval
Statistics	max. and min. values for each jitter measurement type	
Jitter result plots	histogram (rising edges only)	TJ, DJ, DDJ, PJ, RJ+OBUJ
	histogram (falling edges only)	TJ, DJ, DDJ, PJ, RJ+OBUJ
	histogram (both edges)	TJ, DJ, DDJ, PJ, RJ+OBUJ
	TIE track	TJ, DDJ, PJ, RJ+OBUJ
	power spectral density (PSD)	TJ, DDJ, PJ, RJ+OBUJ
Additional result plots	step response	
	bathtub	PJ and (O)BUJ removable from noise bathtub
	synthetic eye diagram	DD only, DD+P(h), DD+P(v), DD+P
	reconstructed signal	composite signal of calculated jitter and noise measurement values
	error signal	difference signal of original input signal and reconstructed signal

R&S®RTP-K134 advanced jitter and noise analysis

General description	The R&S®RTP-K134 option provides advanced jitter and noise measurements and separation. R&S®RTP-K134 option includes R&S®RTP-K133 advanced jitter analysis option and R&S®RTP-K12 basic jitter analysis option.	
Noise separation	total noise (TN), deterministic noise (DN), data dependent noise (DDN), periodic noise (PN), data dependent noise plus periodic noise (DDN+PN), random noise (RN), (other) bounded uncorrelated noise ((O)BUN), random noise plus other (other) bounded uncorrelated noise (RN+(O)BUN)	
Accepted input signals	clock signals or data signals (NRZ)	
Reference clock	internal clock recovery (PLL first or second order, constant clock or feed forward) or explicit clock signal	
Basic measurements	symbol rate, symbol duration, event count	
Noise measurements	eye height at bit error rate (EN@BER)	absolute or relative, BER value selectable between 10^{-32} and 10^{-1}
	level distortion (LD)	absolute or relative value
	inter symbol interference noise (ISIN)	absolute or relative value
	total noise (TN)	peak-to-peak value and RMS value, absolute or relative
	deterministic noise (DN)	peak-to-peak value and RMS value, absolute or relative
	data dependent noise (DDN)	peak-to-peak value and RMS value, absolute or relative
	periodic noise (PN)	peak-to-peak value and RMS value, absolute or relative
	data dependent noise plus periodic noise (DDN+PN)	peak-to-peak value and RMS value, absolute or relative
	periodic noise components	amplitude, frequency, direction (vertical or horizontal)
	random noise (RN)	RMS value, absolute or relative
	(other) bounded uncorrelated noise ((O)BUN)	peak-to-peak value and RMS value, absolute or relative
	(other) bounded uncorrelated noise ((O)BUN, dual-dirac),	absolute or relative value
	random noise plus (other) bounded uncorrelated noise (RJ+(O)BUN)	peak-to-peak value and RMS value, absolute or relative
Statistics	max. and min. values for each noise measurement type	
Noise result plots	histogram (level 0)	TN, DN, DDN, PN, RN+OBUN
	histogram (level 1)	TN, DN, DDN, PN, RN+OBUN
	histogram (both levels)	TN, DN, DDN, PN, RN+OBUN
	TIE track	TN, DDN, PN, RN+OBUN
	power spectral density (PSD)	TN, DDN, PN, RN+OBUN
Additional result plots	step responses	
	noise bathtub	PN and (O)BUN removable from noise bathtub
	synthetic eye diagram	DD only, DD+P(h), DD+P(v), DD+P
	reconstructed signal	composite signal of calculated jitter and noise measurement values
	error signal	difference signal of original input signal and reconstructed signal

R&S®RTP-K135 PAM-N analysis

General description	The R&S®RTP-K135 option extends R&S®RTP-K133 advanced jitter analysis, R&S®RTP-K134 advanced jitter and noise analysis, R&S®RTP-K136 advanced eye analysis (8 Gbps) and R&S®RTP-K137 advanced eye analysis (16 Gbps) for pulse amplitude modulated (PAM) signals up to PAM order 8.	
Signal configuration	number of PAM-N input signal sources	up to 8; independently configurable in technology, serial standard, PAM order and symbol rate
	main sources	analog channels, differential channels, math channels and reference channels
Timing references	advanced jitter and noise analysis	
	explicit clock	NRZ signal
	internal software clock recovery	up to 32 GBaud (depending on device bandwidth)
	advanced eye analysis	
	explicit clock	NRZ signal
	internal software clock recovery	up to 32 GBaud (depending on device bandwidth)
	internal hardware clock recovery	up to 3.8 GBaud
Measurements	advanced jitter and noise analysis	
	basic	see R&S®RTP-K133/-K134
	jitter	see R&S®RTP-K133 incl. all possible level transitions up to PAM level 8
	noise	see R&S®RTP-K134 incl. all possible signal levels up to PAM level 8
	statistics	maximum and minimum for each basic, jitter and noise measurement
	presets	all selected components with explicit level height, one selected component with same level heights or one selected component with same base level
	advanced eye analysis	
	eye	amplitude, rise time, fall time, slew rate rising, slew rate falling and signal levels
	statistics	maximum, minimum, mean, standard deviation, RMS and measurement count for each eye measurement
	presets	depending on additional filters whole, specific or selected eye
Result plots	advanced jitter and noise analysis	
	histogram	see R&S®RTP-K133/-K134 incl. all possible level transitions up to PAM level 8
	track	see R&S®RTP-K133/-K134 incl. all possible signal levels up to PAM level 8
	advanced eye analysis	
	eye diagram	eye with N-1 eye openings
Additional result plots	advanced jitter and noise analysis	
	jitter bathtub	see R&S®RTP-K133
	noise bathtub	see R&S®RTP-K13 incl. N-1 valleys
Additional filters	advanced eye analysis	
	whole eye	N-1 eye openings with all level transitions
	specific eye	one explicit eye opening with all involved level transitions
	selected eye	an explicit eye opening with only its own level transition

R&S®RTP-K136 advanced eye analysis (8 Gbps)

General description	The advanced eye analysis allows the user to generate eye diagrams from long multi-period acquisitions of clock signals, hardware-supported clock data recovery up to a bit rate of 8 Gbps, and serial data signals. It allows the fine control of the signal content that contributes to the eye diagram and enables the advanced analysis, measurement, mask test and navigation functions.	
General configuration	number of eye diagram instances	up to 4; independently configurable
	main source	analog channels, differential channels, math channels, reference channels, track channels
	timing reference source	analog channels, differential channels, math channels, reference channels, track channels
	horizontal settings	range, position; expressed in absolute time or relative to user-defined bit rate
Display	persistence	50 ms to 50 s, or infinite
	trace colors	predefined or user-defined color tables
	eye stripe	displays position of eye diagram slices and masks violations time-correlated to the main source waveform; always enabled, for mask tests only, disabled
Qualification	gate	
	position	start, stop; absolute time or relative to display in percent
	coupling	none, cursor, zoom
	signal	
	source	analog channels, math channels, reference channels
	condition	greater than, less than, in range, out of range; relative to selected reference levels
Filter	DDR3/DDR4 protocol (only in combination with option R&S®RTP-K91/-K93)	
	frame type	any, read frame, non-consecutive read frame, write frame, non-consecutive write frame
	error	length
	bit sequence	
	mode	all, level transition, constant level, bit pattern
	bit pattern setup	up to 8 prefix bit and up to 5 suffix bit with respect to central eye diagram bit
Mask testing	mask test results	
	counters	acquisitions, slices, sample hits, slice hits, fail rate
	violation details	number and position of mask violation, expressed as time instant and slice index
	navigation and zoom	use zoom coupling to navigate to violation upon clicking the corresponding table item
CDR trigger	source	analog channels, differential channels
	algorithm	feed forward, constant frequency
	configuration parameters	serial standard, nominal bit rate, bandwidth, relative bandwidth, sampling time
	nominal bit rate	21 kbps to 8 Gbps; supports bit rate estimation
	bandwidth	1/100 to 1/5000 of the nominal bit rate
	sampling time	0.0 to 1.0 UI

R&S®RTP-K137 advanced eye analysis (16 Gbps)

General description	The advanced eye analysis allows the user to generate eye diagrams from long multi-period acquisitions of clock signals, hardware-supported clock data recovery up to a bit rate of 16 Gbps and serial data signals. It allows the fine control of the signal content that contributes to the eye diagram and enables the advanced analysis, measurement, mask test and navigation functions.	
General configuration	number of eye diagram instances	up to 4; independently configurable
	main source	analog channels, differential channels, math channels, reference channels, track channels
	timing reference source	analog channels, differential channels, math channels, reference channels, track channels
	horizontal settings	range, position; expressed in absolute time or relative to user-defined bit rate
Display	persistence	50 ms to 50 s, or infinite
	trace colors	predefined or user-defined color tables
	eye stripe	displays position of eye diagram slices and masks violations time-correlated to the main source waveform; always enabled, for mask tests only, disabled
Qualification	gate	
	position	start, stop; absolute time or relative to display in percent
	coupling	none, cursor, zoom
	signal	
	source	analog channels, math channels, reference channels
	condition	greater than, less than, in range, out of range; relative to selected reference levels
Filter	DDR3/DDR4 protocol (only in combination with option R&S®RTP-K91/-K93)	
	frame type	any, read frame, non-consecutive read frame, write frame, non-consecutive write frame
	error	length
	bit sequence	
	mode	all, level transition, constant level, bit pattern
	bit pattern setup	up to 8 prefix bit and up to 5 suffix bit with respect to central eye diagram bit
Mask testing	mask test results	
	counters	acquisitions, slices, sample hits, slice hits, fail rate
	violation details	number and position of mask violation, expressed as time instant and slice index
	navigation and zoom	use zoom coupling to navigate to violation upon clicking the corresponding table item
CDR trigger	source	analog channels, differential channels
	algorithm	feed forward, constant frequency
	configuration parameters	serial standard, nominal bit rate, bandwidth, relative bandwidth, sampling time
	nominal bit rate	21 kbps to 16 Gbps; supports bit rate estimation
	bandwidth	1/100 to 1/5000 of the nominal bit rate
	sampling time	0.0 to 1.0 UI

R&S®RTP-K140 high speed serial pattern trigger (8 Gbps)

General description	The R&S®RTP-K140 high speed serial pattern trigger option provides triggering functions for simple or complex combinations of bit patterns or 8b10b words up to a bit rate of 8 Gbps including clock data recovery.	
Source	data	any analog channel
	clock	any analog channel or extracted from data channel by using a clock data recovery
Trigger types	single bit pattern	up to 160 bit; wildcards supported
	dual bit pattern	two bit patterns with 160 bit each connected with logical OR; wildcards supported
	complex word pattern	frame alignment by bit pattern of up to 32 bit or timeout; up to 4 bit patterns (up to 160 bit in total) connected with logical AND or OR; conditions: =, ≠, <, >, ≥, ≤, in range, out of range; bit offset, length and search range definable for each pattern
	8b10b	aligns on selectable comma symbol; trigger condition of up to 16 K/D symbols including wildcards; disparity error, symbol error
	PRBS error	locks to PRBS sequences of type 7, 9, 11, 15, 16, 17, 20, 23, 29, 31 and triggers on error
Clock data recovery	bit rate	21 kbps to 8 Gbps; supports bit rate estimation
	unit interval position	0 to 1

R&S®RTP-K141 high speed serial pattern trigger (16 Gbps)

General description	The R&S®RTP-K141 high speed serial pattern trigger option provides triggering functions for simple or complex combinations of bit patterns or 8b10b words up to a bit rate of 16 Gbps including clock data recovery.	
Source	data	any analog channel
	clock	any analog channel or extracted from data channel by using a clock data recovery
Trigger types	single bit pattern	up to 160 bit; wildcards supported
	dual bit pattern	two bit patterns with 160 bit each connected with logical OR; wildcards supported
	complex word pattern	frame alignment by bit pattern of up to 32 bit or timeout; up to 4 bit patterns (up to 160 bit in total) connected with logical AND or OR; conditions: =, ≠, <, >, ≥, ≤, in range, out of range; bit offset, length and search range definable for each pattern
	8b10b	aligns on selectable comma symbol; trigger condition of up to 16 K/D symbols including wildcards; disparity error, symbol error
	PRBS error	locks to PRBS sequences of type 7, 9, 11, 15, 16, 17, 20, 23, 29, 31 and triggers on error
	128b132b	aligns on selectable word; triggers on selectable word
Clock data recovery	bit rate	21 kbps to 16 Gbps; supports bit rate estimation
	unit interval position	0 to 1

R&S®RTP-K553 external frontend control

General description	The R&S®RTP-K553 external frontend control option enables the use of Rohde & Schwarz external frontends in combination with the R&S®RTP oscilloscope (≥ 8 GHz respectively ≥ 13 GHz bandwidth).	
Supported frontends	R&S®RTP084B, R&S®RTP134B or R&S®RTP164B	• R&S®FE44S • R&S®FE50DTR
	R&S®RTP134B or R&S®RTP164B	• R&S®FE110SR • R&S®FE170SR
Number of channels/frontends	R&S®FE44S, with bandwidth ≤ 1 GHz	4
	R&S®FE50DTR, with bandwidth ≤ 1 GHz	4
	R&S®FE110SR, with bandwidth ≤ 10 GHz	2
	R&S®FE170SR, with bandwidth ≤ 10 GHz	2
Reference frequency	10 MHz	Ref Out
Recommended software options	At least one of these options is required to get a corrected frequency response.	
	I/Q samples	R&S®RTP-K11 I/Q software interface
	real samples	R&S®RTP-K121, deembedding option

Ordering information

Designation	Type	Order No.
Base unit (including standard accessories: R&S®RT-ZA16 precision BNC to SMA adapter (2 pieces), quick start guide, power cord)		
High-performance oscilloscope		
4 GHz, 100 Mpoints memory	R&S®RTP044B	1803.7000.04
6 GHz, 100 Mpoints memory	R&S®RTP064B	1803.7000.06
8 GHz, 100 Mpoints memory	R&S®RTP084B	1803.7000.08
13 GHz, 100 Mpoints memory	R&S®RTP134B	1803.7000.13
16 GHz, 100 Mpoints memory	R&S®RTP164B	1803.7000.16
Hardware options (plug-in)		
Mixed signal option, 400 MHz, 5 Gsample/s, 16 channels	R&S®RTP-B1	1333.2424.02
Digital extension port for R&S®RT-ZVC usage with R&S®RTP oscilloscope, included in R&S®RTP-B1	R&S®RTP-B1E	1337.9581.02
Arbitrary waveform generator, 100 MHz, 2 analog channels, 8-bit pattern generator	R&S®RTP-B6	1333.2418.02
16 GHz differential pulse source	R&S®RTP-B7	1333.2001.02
Additional solid state disk	R&S®RTP-B19B	1803.6855.02
Memory upgrade, 200 Mpoints per channel	R&S®RTP-B102	1337.9517.02
Memory upgrade, 500 Mpoints per channel	R&S®RTP-B105	1337.9523.02
Memory upgrade, 1 Gpoints per channel	R&S®RTP-B110	1337.9530.02
Memory upgrade, 2 Gpoints per channel	R&S®RTP-B120	1803.6455.02
Memory upgrade, 3 Gpoints per channel	R&S®RTP-B130	1803.6610.02
Bandwidth upgrades [14]		
Upgrade of the R&S®RTP044B to 6 GHz bandwidth	R&S®RTP-B0406	1803.6261.02
Upgrade of the R&S®RTP044B to 8 GHz bandwidth	R&S®RTP-B0408	1803.6278.02
Upgrade of the R&S®RTP044B to 13 GHz bandwidth	R&S®RTP-B0413	1803.6284.02
Upgrade of the R&S®RTP044B to 16 GHz bandwidth	R&S®RTP-B0416	1803.6290.02
Upgrade of the R&S®RTP064B to 8 GHz bandwidth	R&S®RTP-B0608	1803.6303.02
Upgrade of the R&S®RTP064B to 13 GHz bandwidth	R&S®RTP-B0613	1803.6310.02
Upgrade of the R&S®RTP064B to 16 GHz bandwidth	R&S®RTP-B0616	1803.6326.02
Upgrade of the R&S®RTP084B to 13 GHz bandwidth	R&S®RTP-B0813	1803.6332.02
Upgrade of the R&S®RTP084B to 16 GHz bandwidth	R&S®RTP-B0816	1803.6349.02
Upgrade of the R&S®RTP134B to 16 GHz bandwidth	R&S®RTP-B1316	1803.6355.02
Software options		
Serial triggering and decoding		
I^2C/SPI serial triggering and decoding	R&S®RTP-K1	1337.8604.02
UART/RS-232/RS-422/RS-485 serial triggering and decoding	R&S®RTP-K2	1337.8610.02
CAN/LIN serial triggering and decoding	R&S®RTP-K3	1337.8627.02
MIL-STD-1553 serial triggering and decoding	R&S®RTP-K6	1800.6654.02
ARINC 429 serial triggering and decoding	R&S®RTP-K7	1800.6660.02
Ethernet (10BASE-T/100BASE-TX) serial triggering and decoding	R&S®RTP-K8	1337.8633.02
CAN-FD serial triggering and decoding	R&S®RTP-K9	1337.8640.02
MIPI RFFE serial triggering and decoding	R&S®RTP-K40	1337.8733.02
MIPI D-PHY serial triggering and decoding	R&S®RTP-K42	1337.8740.02
MIPI M-PHY serial triggering and decoding	R&S®RTP-K44	1337.8756.02
Manchester and NRZ serial triggering and decoding	R&S®RTP-K50	1337.8762.02
8b10b serial triggering and decoding	R&S®RTP-K52	1337.8779.02
MDIO serial triggering and decoding	R&S®RTP-K55	1337.8785.02
Ethernet (100BASE-T1) serial triggering and decoding	R&S®RTP-K57	1800.6548.02
Ethernet (1000BASE-T1) serial triggering and decoding	R&S®RTP-K58	1800.6702.02
USB 1.0/1.1/2.0 serial triggering and decoding	R&S®RTP-K60	1337.8791.02
USB 3.1 Gen 1 serial triggering and decoding	R&S®RTP-K61	1337.8804.02
USB 3.1 Gen 2 serial triggering and decoding	R&S®RTP-K62	1337.9100.02
USB power delivery serial triggering and decoding	R&S®RTP-K63	1337.8810.02
USB 3.1 SSIC serial triggering and decoding	R&S®RTP-K64	1337.9117.02
SpaceWire serial triggering and decoding	R&S®RTP-K65	1800.6677.02
PCI Express 1.1/2.0 serial triggering and decoding	R&S®RTP-K72	1337.8827.02
PCI Express 3.0 serial triggering and decoding	R&S®RTP-K73	1800.6960.02
Low speed serial buses, triggering and decoding (R&S®RTP-K1/-K2/-K50)	R&S®RTP-K510	1803.6632.02
Automotive protocols, triggering and decoding (R&S®RTP-K3/-K9)	R&S®RTP-K520	1803.6649.02
Aerospace protocols, triggering and decoding (R&S®RTP-K6/-K7/-K65)	R&S®RTP-K530	1803.6655.02
Ethernet protocols, triggering and decoding (R&S®RTP-K8/-K55)	R&S®RTP-K540	1803.6661.02
MIPI low speed, triggering and decoding (R&S®RTP-K40)	R&S®RTP-K550	1803.6678.02

[14] The bandwidth upgrade is performed at a Rohde & Schwarz service center, where the oscilloscope will also be calibrated.

Designation	Type	Order No.
Automotive Ethernet, triggering and decoding (R&S®RTP-K57/-K58)	R&S®RTP-K560	1803.6684.02
USB protocols, triggering and decoding (R&S®RTP-K60/-K61/-K62/-K63/-K64)	R&S®RTP-K570	1803.6690.02
MIPI high speed, triggering and decoding (R&S®RTP-K42/-K44)	R&S®RTP-K580	1803.6703.02
PCI express, triggering and decoding (R&S®RTP-K52/-K72/-K73)	R&S®RTP-K590	1803.6710.02
Generic decode (R&S®RTP-K50/-K52)	R&S®RTP-K600	1803.6726.02
Low speed trigger and decode bundle (R&S®RTP-K500/-K510/-K520/-K530/-K540/-K550/-K600)	R&S®RTP-TDBDL1	1803.6732.02
High speed trigger and decode bundle (R&S®RTP-K560/-K570/-K580/-K590)	R&S®RTP-TDBDL2	1803.6749.02
Triggering and decoding bundle ALL (R&S®RTP-K500/-K510/-K520/-K530/-K540/-K550/-K560/-K570/-K580/-K590/-K600)	R&S®RTP-ALLTD	1803.6984.02
Compliance tests		
USB 2.0 compliance test	R&S®RTP-K21	1337.8685.02
Ethernet compliance test (10/100/1000BASE-T/EEE)	R&S®RTP-K22	1337.8691.02
Ethernet compliance test (2.5/5/10GBASE-T)	R&S®RTP-K23	1337.8704.02
Ethernet compliance test (100BASE-T1)	R&S®RTP-K24	1800.6531.02
MIPI D-PHY compliance test	R&S®RTP-K26	1337.8727.02
MIPI D-PHY 2.5 compliance test	R&S®RTP-K27	1800.5993.02
MIPI C-PHY 2.1 compliance test	R&S®RTP-K28	1802.9621.02
PCI Express 1.1/2.0 compliance test	R&S®RTP-K81	1337.8885.02
PCI Express 1.1/2.0/3.0 compliance test	R&S®RTP-K83	1800.6954.02
Ethernet compliance test (1000BASE-T1)	R&S®RTP-K87	1800.6554.02
Ethernet compliance test (MGBASE-T1)	R&S®RTP-K88	1800.6725.02
Ethernet compliance test (10BASE-T1)	R&S®RTP-K89	1800.6719.02
DDR3/DDR3L/LPDDR3 signal integrity debugging and compliance test	R&S®RTP-K91	1337.8840.02
eMMC compliance test	R&S®RTP-K92	1803.6378.02
DDR4/LPDDR4 signal integrity debugging and compliance test	R&S®RTP-K93	1801.3671.02
DDR5 signal integrity debugging and compliance test	R&S®RTP-K94	1803.6926.02
LPDDR5 signal integrity debugging and compliance test	R&S®RTP-K95	1803.7045.02
R&S®ScopeSuite automation	R&S®RTP-K99	1326.4425.02
USB 3.2 transmitter compliance test	R&S®RTP-K101	1800.6948.02
USB 3.2 receiver compliance test	R&S®RTP-K102	1800.6990.02
HDMI 1.4/2.1 TMDS compliance test	R&S®RTP-K110	1802.9467.02
DisplayPort (DP) 1.4a compliance test	R&S®RTP-K114	1803.6903.02
Embedded DisplayPort (eDP) 1.4b/1.5 compliance test	R&S®RTP-K115	1803.6910.02
Analysis		
I/Q software interface	R&S®RTP-K11	1800.6683.02
Jitter analysis	R&S®RTP-K12	1337.8656.02
Zone trigger	R&S®RTP-K19	1337.8879.02
Bus analysis	R&S®RTP-K35	1800.6648.02
Spectrogram	R&S®RTP-K37	1338.1110.02
User-defined math	R&S®RTP-K39	1803.6761.02
Modulated load pull	R&S®RTP-K98	1803.6990.02
Deembedding base option	R&S®RTP-K121	1326.3064.02
Realtime deembedding extension	R&S®RTP-K122	1326.3070.02
Embedding and equalization	R&S®RTP-K126	1800.6025.02
Video raster analysis	R&S®RTP-K129	1803.7068.02
TDR/TDT analysis	R&S®RTP-K130	1326.3093.02
Advanced jitter analysis	R&S®RTP-K133	1800.6860.02
Advanced jitter and noise analysis	R&S®RTP-K134	1800.6977.02
PAM analysis	R&S®RTP-K135	1803.6861.02
Advanced eye analysis (8 Gbps)	R&S®RTP-K136	1803.6561.02
Advanced eye analysis (16 Gbps)	R&S®RTP-K137	1800.6983.02
High speed serial pattern trigger (8 Gbps)	R&S®RTP-K140	1326.4554.02
High speed serial pattern trigger (16 Gbps)	R&S®RTP-K141	1326.4560.02
Bus analysis (R&S®RTP-K35)	R&S®RTP-K500	1803.6626.02
External frontend control	R&S®RTP-K553	1803.6890.02
Signal integrity bundle 1 (R&S®RTP-K12/-K19/-K121/-K122/-K141)	R&S®RTP-SIBDL1	1803.6755.02
Signal integrity bundle 2 (R&S®RTP-K126/-K134/-K135/-K137)	R&S®RTP-SIBDL2	1800.7309.02
Signal integrity bundle ALL (R&S®RTP-K19/-K121/-K122-K126/-K134/-K135/-K137/-K14)	R&S®RTP-ALLSI	1800.7315.02

Designation	Type	Order No.
Probes		
8.0 GHz transmission line probe, 10:1, 500 Ω, 0.3 pF, 20 V (RMS)	R&S®RT-ZZ80	1409.7608.02
3.0 GHz active voltage probe, single-ended, 1 MΩ, 0.8 pF	R&S®RT-ZS30	1410.4309.02
6.0 GHz active voltage probe, single-ended, 1 MΩ, 0.3 pF	R&S®RT-ZS60	1418.7307.02
4.0 GHz power rail probe, 1:1, low noise, 50 kΩ, large offset range ±60 V	R&S®RT-ZPR40	1800.5406.02
1.0 GHz active voltage probe, differential, 1 MΩ, 0.6 pF, incl. R&S®RT-ZA15	R&S®RT-ZD10	1410.4715.02
1.5 GHz active voltage probe, differential, 1 MΩ, 0.6 pF	R&S®RT-ZD20	1410.4409.02
3.0 GHz active voltage probe, differential, 1 MΩ, 0.6 pF	R&S®RT-ZD30	1410.4609.02
4.5 GHz active voltage probe, differential, 1 MΩ, 0.4 pF	R&S®RT-ZD40	1410.5205.02
6.0 GHz modular probe amplifier, differential, 400 kΩ, multimode	R&S®RT-ZM60	1419.3105.02
9.0 GHz modular probe amplifier, differential, 400 kΩ, multimode	R&S®RT-ZM90	1419.3205.02
13.0 GHz modular probe amplifier, differential, 400 kΩ, multimode	R&S®RT-ZM130	1800.4500.02
16.0 GHz modular probe amplifier, differential, 400 kΩ, multimode	R&S®RT-ZM160	1800.4600.02
Tip cable, solder in, length: 15 cm, multimode compatible	R&S®RT-ZMA10	1419.4301.02
Tip cable, square pin, for 1.27 mm pin header, length: 15 cm, multimode compatible	R&S®RT-ZMA12	1419.4324.02
Tip cable, quick connect, for solder in resistor connection, length: 15 cm, multimode	R&S®RT-ZMA15	1419.4224.02
Browser module, variable span from 0.5 mm to 8 mm, spring-loaded, multimode	R&S®RT-ZMA30	1419.4353.02
SMA module, 2.92 mm/3.5 mm/SMA, differential, 100 Ω, DC termination, multimode	R&S®RT-ZMA40	1419.4201.02
Extended temperature kit, 1 m matched cable pair, multimode compatible	R&S®RT-ZMA50	1419.4218.02
Multi-channel power probe, 2 × 4 voltage/current channels	R&S®RT-ZVC04	1326.0259.04
Multi-channel power probe, 2 × 2 voltage/current channels	R&S®RT-ZVC02	1326.0259.02
Compact probe set for E and H near-field measurements, 30 MHz to 3 GHz	R&S®HZ-15	1147.2736.02
3 GHz, 20 dB preamplifier, 100 V to 230 V power adapter, for R&S®HZ-15	R&S®HZ-16	1147.2720.02
Probe accessories		
High-impedance buffer amplifier, incl. 500 MHz passive probe	R&S®RT-Z1M	1337.9200.02
Spare accessory set for R&S®RT-ZS10/-ZS10E/-ZS20/-ZS30	R&S®RT-ZA2	1416.0405.02
Pin set for R&S®RT-ZS10/-ZS10E/-ZS20/-ZS30	R&S®RT-ZA3	1416.0411.02
Mini clips	R&S®RT-ZA4	1416.0428.02
Micro clips	R&S®RT-ZA5	1416.0434.02
Lead set	R&S®RT-ZA6	1416.0440.02
Pin set for R&S®RT-ZD20/-ZD30	R&S®RT-ZA7	1417.0609.02
Pin set for R&S®RT-ZD40	R&S®RT-ZA8	1417.0867.02
Probe box to N/USB adapter	R&S®RT-ZA9	1417.0909.02
External attenuator, 10:1, 2.0 GHz, 70 V DC, 46 V AC (peak)	R&S®RT-ZA15	1410.4744.02
Power rail browser kit	R&S®RT-ZA25	1800.5329.00
Pigtail cable, solder-in, length: 15 cm, for R&S®RT-ZPR20	R&S®RT-ZA26	1800.5258.00
3D probe positioner	R&S®RT-ZAP	1326.3641.02
Extended cable set for R&S®RT-ZVC, PCB probing, 1 current and voltage lead, length: 32 cm	R&S®RT-ZA30	1333.1686.02
Extended cable set for R&S®RT-ZVC, 4 mm probing, 1 current and voltage lead, length: 32 cm	R&S®RT-ZA31	1333.1692.02
Oscilloscope interface cable for R&S®RT-ZVC (included in R&S®RT-ZVC02/-ZVC04, 1326.0259.02/.04)	R&S®RT-ZA33	1333.1770.02
Extended cable set for R&S®RT-ZVC, 4 mm probing, 1 current and voltage lead, length: 1 m	R&S®RT-ZA34	1333.1892.02
Extended cable set for R&S®RT-ZVC, PCB probing, 1 current and voltage lead, length: 1 m	R&S®RT-ZA35	1333.1905.02
Solder-in cable set for R&S®RT-ZVC, 4 current and voltage solder-in cables, solder-in pins	R&S®RT-ZA36	1333.1911.02
Extended cable set for R&S®RT-ZVC, BNC connector, 1 current and voltage lead, length: 16 cm	R&S®RT-ZA37	1337.9130.02
Adapter, Rohde & Schwarz probe interface to 2.92 mm/3.5 mm/SMA, incl. USB-C port	R&S®RT-ZA50	1803.5265.02
Adapter, 2.92 mm/3.5 mm/SMA to Rohde & Schwarz probe interface, incl. USB-C port	R&S®RT-ZA51	1803.5365.02

Designation	Type	Order No.
Accessories		
Precision BNC to SMA adapter	R&S®RT-ZA16	1320.7074.02
Matched pair cable	R&S®RT-ZA17	1337.8991.02
Front cover, for R&S®RTP oscilloscopes	R&S®RTP-Z1	1337.9569.02
Front handles, for R&S®RTP oscilloscopes	R&S®RTP-B20B	1803.6410.02
Transit case, for R&S®RTP oscilloscopes	R&S®RTP-Z4	1801.4610.02
USB 2.0 compliance test fixture set	R&S®RT-ZF1	1317.3420.02
Ethernet compliance test fixture set	R&S®RT-ZF2	1317.5522.02
Ethernet 1000BASE-T1 jitter test cable	R&S®RT-ZF2C	1317.5639.02
Frequency converter (100BASE-T1)	R&S®RT-ZF3	5025.0670.02
Ethernet 10BASE-Te fixture	R&S®RT-ZF4	1333.0915.02
Ethernet probe fixture	R&S®RT-ZF5	1333.0938.02
Frequency converter (1000BASE-T1)	R&S®RT-ZF6	1337.8579.02
Automotive Ethernet T&D fixture	R&S®RT-ZF7	1801.3688.02
SMA adapter	R&S®RT-ZF7A	1801.4126.02
SMA adapter, for PoDL	R&S®RT-ZF7P	1802.9680.02
Automotive Ethernet compliance fixture	R&S®RT-ZF8	1801.3694.02
Probe deskew and calibration test fixture	R&S®RT-ZF20	1800.0004.02
Probe test fixture	R&S®RT-ZF30	1333.2099.02
19" rackmount kit, for R&S®RTP oscilloscopes, 6 HU resulting height	R&S®ZZA-KN6	1175.3056.00

Warranty and service

Warranty		
Base unit		1 year
All other items		1 year
Service options		
	Service plans	**On demand**
Calibration	up to five years [15]	pay per calibration
Warranty and repair	up to five years [15]	standard price repair
Contact your Rohde & Schwarz sales office for further details.		

[15] For extended periods, contact your Rohde & Schwarz sales office.

Service at Rohde&Schwarz
You're in great hands

- Worldwide
- Local and personalized
- Customized and flexible
- Uncompromising quality
- Long-term dependability

Rohde&Schwarz

The Rohde&Schwarz technology group is among the trailblazers when it comes to paving the way for a safer and connected world with its leading solutions in test&measurement, technology systems and networks&cybersecurity. Founded more than 90 years ago, the group is a reliable partner for industry and government customers around the globe. The independent company is headquartered in Munich, Germany and has an extensive sales and service network with locations in more than 70 countries.

www.rohde-schwarz.com

Sustainable product design

- Environmental compatibility and eco-footprint
- Energy efficiency and low emissions
- Longevity and optimized total cost of ownership

Certified Quality Management
ISO 9001

Certified Environmental Management
ISO 14001

More certificates of Rohde&Schwarz

Rohde&Schwarz training
www.training.rohde-schwarz.com

Rohde&Schwarz customer support
www.rohde-schwarz.com/support

PD 3683.5616.22 | Version 12.00 | June 2025 (sk)
R&S®RTP High-Performance Oscilloscope